Radio Shack®

Service Manual

26-6001/2

TRS-80®

Model 16

Catalog Number 26-6001/2

CUSTOM MANUFACTURED IN U.S.A. BY RADIO SHACK, A DIVISION OF TANDY CORPORATION

TRS-8Ø® Model 16 Service Manual

Contents

Introduction

The TRS-8Ø Model 16 contains two microprocessors -- the MC68ØØØ and the Z-8ØA. This allows both 8-bit and 16-bit selectable operation.

This manual will provide information primarily on the 68ØØØ side of the Model 16. For Z-8Ø information that has not been included, refer to the Model II Technical Reference Manual or the Model II Service Manual.

1/ Technical Specifications

Processor Modules

The TRS-8Ø® Model 16 is a dual processor system. One processor is dedicated to Input/Output tasks, while the other is dedicated to high-level language tasks.

MC68ØØØ CPU Board

The MC68ØØØ CPU Board:

- Provides 16-bit operation for high-level language tasks.
- Supports direct access for up to 7 megabytes of memory.
- Supports 8 levels of vectored interrupts.
- Supports 4 levels of fixed priority bus arbitration.
- Supports a Z8Ø to MC68ØØØ memory interface controller.

The major components of the MC68ØØØ CPU Board include the:

- MC68ØØØ CPU.
- AM9519A Interrupt Controller.

128K/256K-Byte Memory Board

The 128K-byte Memory Board provides:

- Space where an optional 128K-bytes of memory can be installed.
- Optional byte parity checking and detection logic.
- Option selecting to map memory on any 256K boundary within 7-Meg memory space.

Z8Ø CPU Board

The Z8Ø CPU Board:

- Provides primary DMA channel -- memory to memory, I/O to memory, or memory to I/O.
- Supports Z8Ø Mode 2 vectored interrupts.
- Supports dual RS-232 Interfaces.
- Supports both asynchronous and synchronous communication schemes.
- Provides boot-strap firmware which resides in the lower 2K of the 64K address space. (Boot-strap firmware is switched out of the address space after bootup is complete.)

The major components of the CPU Board include:

- Z8Ø-A CPU.
- Z8Ø-A CTC.
- Z8Ø-A DMA.
- Z8Ø-A SIO.

Floppy Disk Controller/Printer Interface Board

The Floppy Disk Controller (FDC) Board provides:

- Software-selectable double- or single-density operation.
- Two independent drive interfaces, one for the internal drives and one for the external drives.
- Adjustable write pre-compensation from Ø ns to 35Ø ns.
- Fast parallel printer interface, capable of generating an interrupt when the printer can accept another character.

The major components of the FDC Board include:

- Z8Ø-A PIO.
- WD1791.
- WD1691.
- WD2143.

64K-byte Memory Board

The 64K-byte Memory Board provides jumper option selection for one of 15 memory pages.

Its major components are 4116 16K x 1 dynamic RAMs.

Video/Keyboard Interface Board

The Video/Keyboard Interface Board provides:

- 24 lines of either 8Ø or 4Ø characters.
- Programmable timing parameters.
- Serial bit stream, processor interrupt.

Its major components are an MC6845 CRT controller and 2114 static RAMs.

Motherboard (8-slot)

The 8-slot Motherboard provides 8Ø conductor paths which distribute regulated power and provide signal interconnection for the system boards.

Optional Boards

Optional boards include the following:

- Hard Disk Interface Board -- 16K RAM, bank-selectable. Interfaces to intelligent high-speed controller. 1 to 4 hard disk drives supported. Major components include 4116 16K-by-1 dynamic RAMs, Z8Ø-A CTC.

- High-Resolution Graphics Board -- 64Ø x 24Ø-pixel resolution. Direct overlay of alphanumerics and auto reverse. Options: Register user-programmable for blanking graphics, selecting wait states, and controlling the X and Y address pointers. Option: Control and Data Registers are port mapped. Address pointers increment or decrement automatically after a read or write of memory. Major components include 4116 16K-by-1 dynamic RAMs.

- Arcnet Interface Board -- Local Area Network supports up to 255 users on the same network with a transmission capability of up to 2ØØØ feet and a data rate of 2.5

M-bits. Buffer Memory is segmented into four pages of 256 bytes each. Its major components include a custom LSI device and 2114 static RAMs.

128K/256K Memory Board -- 128K or 256K-bytes of dynamic RAM, depending upon whether one or two RAM banks have been installed. Byte parity checking and detection logic is also provided as an option. The 128K/256K Memory Board's major components include MCM6665 64K-by-1 dynamic RAMs.

CRT Display Module

The CRT display module has basically the same specifications as the Model II video monitor; however, increased bandwidth (22 MHz) is provided for a sharper display. Resolution is typically 9ØØ lines at center screen and 75Ø lines in the corners. A green P5 phosphor CRT is provided.

Floppy Disk Drives

The Model 16 can have one or two Tandon Thin-Line drives, double- or single-sided media, single- or double-density, built into the Computer.

Power Supply

The power supply requirements are:

- +5v @ 13.36 A.
- +12v @ 2.5 A.
- -12v @ 2ØØ MA.
- +24v @ 1.7 A.

2/ Theory of Operation

Model 16 CPU Board Theory of Operation

The theory of operation for the CPU board has been broken up into several major sections, each corresponding to a logical unit of LSI, MSI, and SSI parts on the CPU board. They are as follows:

- Section 1.0 Central Processing Unit (CPU)
- Section 2.0 Interrupt Logic
- Section 3.0 Z80 to 68000 Memory Interface Circuitry
- Section 4.0 Memory Management Circuitry
- Section 5.0 Bus Arbitration Logic
- Section 6.0 Data Transfer Acknowledge Logic
- Section 7.0 68000 I/O Decoding and Strobes
- Section 8.0 Clock Logic
- Section 9.0 Refresh Logic
- Section 10.0 Bus Error Logic

Note: The terms "assertion" and "negation" are used to avoid confusion when talking about active-high or active-low signals. "Assert" or "assertion" is used to indicate a true or active state, regardless of its high or low potential. "Negate" or "negation" indicates a false or inactive state.

Section 1.0 Central Processing Unit (CPU)

The Model 16 board uses the Motorola MC68000 chip which contains 16 data lines, 23 address lines, and 20 control lines.

The data lines (KD0-KD15) are interfaced to the bus via tranceivers U15 and U16 (AMD 8303's). When high, the CD control line (pin 9) on the transceivers tri-states the data bus. This signal is driven by Bus Grant Acknowledge (BGACK), which indicates that a device other than the 68000 CPU is bus master.

The TR control line (pin 11 on the 83Ø3's) controls the direction the transceiver is pointing and is driven by Data Bus Transmit/Receive (DBTR). (See the upper left-hand corner of Sheet 3 of the CPU schematic.) The active-low output DBTR from U4Ø pin 1Ø enables the data receivers during an off-board interrupt acknowledge sequence (INTAKL6*) or during a read from external memory.

The active-high state of DBTR enables the data drivers. It, therefore, follows that the data receivers are disabled when:

- A read or write is in progress from the Interrupt Controller chip (INTCS*).
- A board interrupt acknowledge sequence is in progress (PRIORINTAK*).
- A write to external memory (R/W*) occurs.

It should be noted that the CD control line overrides the TR control line, and that both drivers and receivers are disabled (tri-stated) if BGACK is asserted.

Address Lines

The 68ØØØ address lines are interfaced to the address bus via tranceivers U14, U33, and U44, which are the same type used for the data lines. The CD control line is connected directly to ground which always enables address lines KA1-KA11, EA12-EA19, and KA2Ø-KA23 to the address bus.

The direction control line (TR) is switched by BGACK* which indicates who has bus mastership. If the 68ØØØ CPU is bus master, then BGACK* is negated and the address lines are driven onto the bus. If an external device is bus master, BGACK* will be asserted and the address contained on the bus will be gated onto the CPU address lines.

The control lines are contained in six major groups. These are:

- Memory Access Control Lines.
- Bus Arbitration Lines.
- Interrupt Priority Lines.
- Function Code Lines.
- 68ØØ Peripheral Interface Lines.
- System Control Lines.

Memory Access Control Lines

The memory access control lines include Address Strobe (AS*), Lower Data Strobe (LDS*), Upper Data Strobe (UDS*), Read/Write (R/W*), and Data Transfer Acknowledge (DTACK*). AS* indicates there is a valid address on the address lines of the 68ØØØ CPU and it is connected directly to the 68ØØØ subsystem devices.

The Bus AS* (BAS*) depends upon the state of the 68ØØØ CPU. When the processor is in the user state, a delayed AS* is required to allow the extra time needed for address checking of the memory management unit. The logic described on Sheet 3 of the CPU schematic (lower left-hand corner) steers AS* or MAS (the delayed AS* for user state) to GAS* which is interfaced to the bus by U18.

LDS*, UDS*, and R/W* are directly interfaced to the bus using a non-inverting tranceiver -- U18 (AMD 81Ø4). The control lines are the same as described for the AMD 83Ø3 (the address and data transceivers). The TR input for U18 is pulled up which always enables the drivers, while the CD input is controlled by BGACK which will disable (tri-state) the drivers when an external device is bus master.

LDS* indicates that data bits BDØ-BD7 are being accessed, and UDS* indicates that data bits BD8-BD15 are being accessed. If both are asserted at the same time, all 16 data bits are accessed. R/W* indicates whether the data bus transfer is a read or write cycle. An active high indicates a read cycle and an active low indicates a write.

Data Transfer Acknowledge (DTACK*) is the asynchronous handshake signal used by memory and peripheral devices to indicate that a bus cycle has been completed. DTACK* is connected directly to the bus and becomes BDTACK*. For more details, see **Section 6.Ø Data Transfer Acknowledge Logic.**

Bus Arbitration Lines

The bus arbitration lines consist of Bus Request (BR*), Bus Grant (BG*), and Bus Grant Acknowledge (BGACK*). BR* and BGACK* are inputs to the 68ØØØ CPU and BG* is an output. These signals are used to determine which device will be the next bus master.

All three signals connect with the bus arbitration controller chip (U12). This chip interfaces with the bus to

provide four levels of bus requests and grants. For more details, see **Section 5.Ø Bus Arbitration Logic.**

Interrupt Priority Lines

The Interrupt Priority Lines (IPLØ*-IPL2*) are CPU inputs which indicate the encoded priority of the interrupt-requesting device. The highest priority is Level 7; Level Ø indicates that interrupts are not requested.

IPLØ*-IPL2* are connected to the outputs of an 8-to-3 line priority encoder (U21) whose inputs are the interrupt sources -- either GINT* or MIIINT*. U21 is always enabled with pin 5 (EI) grounded. Level 5 interrupt is the only level currently used. Jumpers E19 and E16 are connected to accomplish this.

For more details on interrupt operation, see **Section 2.Ø Interrupt Logic.**

Function Code Lines

Function Code lines (FCØ, FC1, and FC2) are outputs from the processor chip which feed a 3-to-8 decoder (U6). U6 is used to detect accesses to User Space (either code or data) or to decode the Interrupt Acknowledge sequence (INTAK*).

Bus grant acknowledge (BGACK) disables the decoder to prevent the memory management unit from providing the memory protect function during bus cycles under external control (i.e., Z8Ø, CPU, or DMA transfers).

68ØØ Peripheral Interface Lines

The 68ØØ Peripheral Interface Lines (E, VMA*, and VPA*) allow the CPU to interface easily to 68ØØ-type devices. The outputs (E and VMA*) are interfaced to the 68ØØ bus with a bidirectional transceiver (U18). U18's enable is controlled by the BGACK signal.

The direction of the transceiver is fixed to transmit to the bus. If BGACK is active, the transceiver is disabled and the outputs are tri-stated. Another device is then allowed to drive the bus control lines (i.e., Z8Ø, CPU, or DMA). The 68ØØ Peripheral Interface lines are not currently implemented in the Model 16 operation.

System Control Lines

The System Clock input (CLK) to the 68ØØØ CPU is driven by the 6-MHz output of the clock logic (PCLOCK). The RESET*, HALT*, and BERR* lines are connected directly to the 68ØØØ bus. These lines are driven in a wire-or fashion by open collector inverters (U5Ø). RESET* and HALT* are directly controlled by the Z8Ø CPU. This is done by setting or resetting latched bits in a special Z8Ø I/O port.

RESET* is a bidirectional signal allowing the Z8Ø I/O port latch or the 68ØØØ CPU to reset the 68ØØØ subsystem. For the 68ØØØ CPU to recognize the assertion of RESET*, HALT* must be asserted at the same time.

HALT* is also a bidirectional signal. When the Z8Ø I/O port latch asserts HALT*, the 68ØØØ CPU will stop at the end of the current bus cycle. If HALT* is asserted by the 68ØØØ CPU, it indicates the processor has stopped, as in the case of a double bus fault. See **Section 3.Ø Z8Ø to 68ØØØ Memory Interface Circuitry** for more information.

Assertion of Bus Error (BERR*) to the 68ØØØ CPU indicates that a major error has occurred during the current bus cycle.

Errors can be a result of:

- A device that does not respond with BDTACK*.
- An attempt by the user to access memory outside the extents defined by the memory management unit.
- No interrupt vector received during an interrupt acknowledge sequence.

See **Section 1Ø.Ø Bus Error Logic** for more information.

Section 2.Ø Interrupt Logic

The Interrupt Control function for the 68ØØØ subsystem is implemented with an AM9519 interrupt controller. A single AM9519 manages up to eight maskable interrupt request inputs, resolves priorities, and supplies the vector number response to the 68ØØØ CPU at interrupt acknowledge time. When the AM9519 controller receives an unmasked interrupt request, it issues a group interrupt request to the 68ØØØ CPU. When the interrupt is acknowledged, the controller

outputs the pre-programmed vector number corresponding to the highest-priority unmasked interrupt request.

Operating Mode Register

The mode register in the AM9519 specifies the various combinations of operating options that the programmer may use. The following is a list of the operating options used by the system.

- Priority Mode, selected by mode bit 0.
- Vector Selection, selected by mode bit 1.
- Interrupt Mode, selected by mode bit 2.
- GINT Polarity, selected by mode bit 3.
- IREQ Polarity, selected by mode bit 4.
- Mode bits 5 and 6 select which internal register to be read on a subsequent read operation.
- Mode bit 7 is the master mask bit which enables or disables all interrupts without modifying the interrupt mask register.

Interrupt Request Inputs

Table 1 lists, in order from highest to lowest priority, the interrupt inputs implemented in the 68000 subsystem.

For more information, see the AM9519 data sheet section in the **AM9500 Peripheral Products Guide** published by Advanced Micro Devices.

Section 3.0 Z80 to 68000 Memory Interface Circuitry

Communication between the two CPU's is accomplished with the Z80 CPU initiating interrupts to the 68000, indicating I/O completion, etc. The Z80 CPU can periodically poll a 68000 memory location to recognize requests for service from the 68000.

Optionally, the 68000 can generate an interrupt to the Z80 by accessing a decoded 68000 memory location (not available on Model II/16 upgrades). Once a request for service has been recognized by the Z80 CPU, a descriptor block is read into Z80 memory from 68000 memory to determine the specific service required.

Interrupt	Description	Vector Location
CONT4*	Initiated by the Z8Ø.	234H
CONT5*	Initiated by the Z8Ø.	238H
CONT6*	Initiated by the Z8Ø.	23CH
ADERR*	Address error, generated by the memory management unit when a user attempts memory access outside the defined range.	24ØH
TIMERRI*	Time-out error, generated when no DTACK is received with the 68ØØØ as the bus master.	244H
TMERRE*	Time-out error, generated when no DTACK is received and the 68ØØØ is not the bus master.	248H
IPER*	Parity error, generated on a memory parity error when the 68ØØØ is the bus master.	24CH
EPER*	Parity error, generated on a memory parity error when the 68ØØØ is not the bus master.	25ØH

Table 1. Interrupt Inputs

Prior to attempting a memory transfer by the Z8Ø subsystem to or from the 68ØØØ memory, all Z8Ø memory pages must be deselected by resetting the lower nibble of port ØFFH. This implies that certain precautions must be observed. The stack and control program must be located in the lower 32K of the Z8Ø address space, since page zero cannot be disabled.

Additionally, two control ports must be initialized to determine the addresses involved and the mode of the transfer.

The two ports are described in the tables and text below.

Upper Address Latch (port ØDFH)

Description: Output only, latches the upper address bits (A22-A15) for a Z8Ø transfer to or from 68ØØØ memory.

Data Bit	Function
7	A22
6	A21
5	A2Ø
4	A19
3	A18
2	A17
1	A16
Ø	A15

Transfer Control Latch (port ØDEH)

Description: Output only, latches one address bit and seven control outputs.

Data Bit	Function
7	A14
6	CONT6
5	CONT5
4	CONT4
3	RESET
2	HALT
1	CONT1
Ø	CONTØ

Details of Control Outputs (port ØDEH)

CONTØ
Ø = If Z8Ø AØ = Ø asserts UDS*.
    If Z8Ø AØ = 1 asserts LDS*.
1 = If Z8Ø AØ = Ø asserts LDS*.
    If Z8Ø AØ = 1 asserts UDS*.

CONT1
Ø = Enables Z8Ø to initiate memory transfers to or from 68ØØØ memory space.
1 = Transfers by Z8Ø disabled.

HALT
Ø = 68ØØØ processor not halted.
1 = Halts 68ØØØ processor.

RESET
Ø = RESET negated.
1 = Asserts RESET to 68ØØØ processor.

CONT4
Interrupt to 68ØØØ processor.
Transition generates interrupt.

CONT5
Interrupt to 68ØØØ processor.
Transition generates interrupt.

CONT6
Interrupt to 68ØØØ processor.
Transition generates interrupt.

Section 4.Ø Memory Management Circuitry

A fast memory management scheme provides two sets of offset and limit registers. The offset and limit registers define the relocation base address and the absolute limit address allowed by the current user program. Providing two sets of limit and offset registers allows all user programs to access a common kernel of the operating system or the run-time package.

Memory is allocated in 4K-byte increments and relocation is done on 4K-byte boundaries. Memory management is not active in system mode or during memory transfers initiated by bus masters other than the 68ØØØ CPU.

Write protection for the memory outside a user's partition is provided. Accesses outside of the user's defined partition result in the generation of a bus error exception. An interrupt can also be generated if the interrupt controller is properly initialized.

There are two things that cause the generation of a bus error:

- The user addresses outside his partition.
- A bus time-out occurs.

A bus time-out results when nonexistent memory or I/O accesses are attempted. The source of the bus error can be determined by reading the status register of the interrupt controller.

The hardware which accomplishes the memory management function works as described in the following paragraphs.

68ØØØ processor address bits A12 through A19 are added to the 8-bit value which is stored in the active offset register. The result of this addition is the effective address which is presented to the address bus.

The effective address is compared to the 8-bit value which is stored in the active limit register. If the effective address is larger than the contents of the active limit register, or if the addition results in a carry overflow from the adder, a bus error is generated.

68ØØØ processor address A23 determines which set of offset and limit registers are used. If A23 is high, then offset

and limit registers two will be active; while, if A23 is low, offset and limit registers one will be active.

Each of the two extents is implemented with an offset register and a limit register, which are 74LS374 8-bit D-type registers. The 8-bit value in the offset register is added to the eight processor address lines (KA12 to KA19) to form User Extent Address lines (UEA12 to UEA19).

The effective address is then compared with the value in the limit register; if the EA is greater than the limit, an out-of-bounds error is generated.

A carry out of the adder (LS283) also generates an OBERROR. If OBERROR occurs when MMA and MAS are active, then an Address Error is generated (ADERR). This signal (ADERR) is one of the interrupt sources.

Two 4-bit multiplexors (LS157) select either the processor address (KA12-KA19) or the User Extent Address (UEA12-UEA19) to form the Effective Address (EA12-EA19). MMA selects the address source, and the upper processor address (KA23) selects the active extent.

For a one-megabyte memory space, eight bits of memory management allow 4K minimum granule sizes to be protected.

Note: KA22 asserted selects the I/O device address space. The I/O device strobe generation logic generates the I/O strobes necessary to communicate with interrupt controller and memory management registers by decoding KA21 and KA22.

Section 5.Ø Bus Arbitration Logic

Bus arbitration allows other devices capable of being bus master to request, be granted, and acknowledge bus mastership. The bus arbitration sequence is as follows:

1. The device asserts a Bus Request (BR*).

2. The 68ØØØ CPU asserts a Bus Grant (BG*) to indicate that the bus will be released at the end of the current bus cycle.

3. The device acknowledges the bus grant by asserting a Bus Grant Acknowledge (BGACK*) and assuming bus mastership. A requesting device should not assert BGACK* or assume bus mastership until the following conditions are met:

   - A bus grant has been received.
   - BAS* has been negated, indicating that the CPU has completed the current bus cycle.
   - BDTACK* has been negated, indicating that memory or peripherals are not using the bus.
   - BGACK* has been negated, indicating that no other device still has bus mastership.

4. The device negates the Bus Request (BR*).

The bus arbitration control is performed by the bus arbitration controller chip U12. In addition to controlling the bus arbitration sequence, U12 manages four levels of bus requests and grants.

The sources for the four levels are Refresh Request (REFRQ*), Bus Request 2 (BR2*), Bus Request 1 (BR1*), and Bus Request Ø (BRØ*), with REFRQ* having the highest priority and BRØ* the lowest. The bus requests are pre-latched by a quad-D-type latch U64 clocked at a 12-MHz rate.

The bus request is latched at a Q output of U64 and asserts a bus request input of U12 (pins 3-6). The bus arbitration controller will, in turn, assert BR* to the 68ØØØ CPU. After some internal synchronization time, the 68ØØØ will assert BG* to U12 which indicates that it will release the bus at the end of the current bus cycle.

When the current bus cycle has ended (i.e., when BAS* and BDTACK* are negated), U12 will assert a bus grant to the requesting device with the highest priority. The bus arbitration controller U12 will also assert BGACK* and negate BR* to the 68ØØØ CPU. BGACK* is inverted by 1/6 of U5 and both signals are used to indicate to other bus-controlling circuitry that an external device has become bus master.

The 68ØØØ CPU will negate BG* and wait until BGACK* has been negated before reassuming bus mastership. The requesting device can then assume bus mastership and perform any data transfers needed.

When the current bus master is finished, it negates the bus request to the bus arbitration controller through U64. Then, if there is a bus request still pending, a bus grant will be asserted to the next requesting device and BGACK* will remain asserted until all pending bus requests have been satisfied.

If no bus requests are pending, the bus arbitration controller will negate BGACK* and allow the 68ØØØ CPU to assume bus mastership. See **Figure 1** for the timing relationships of this circuit.

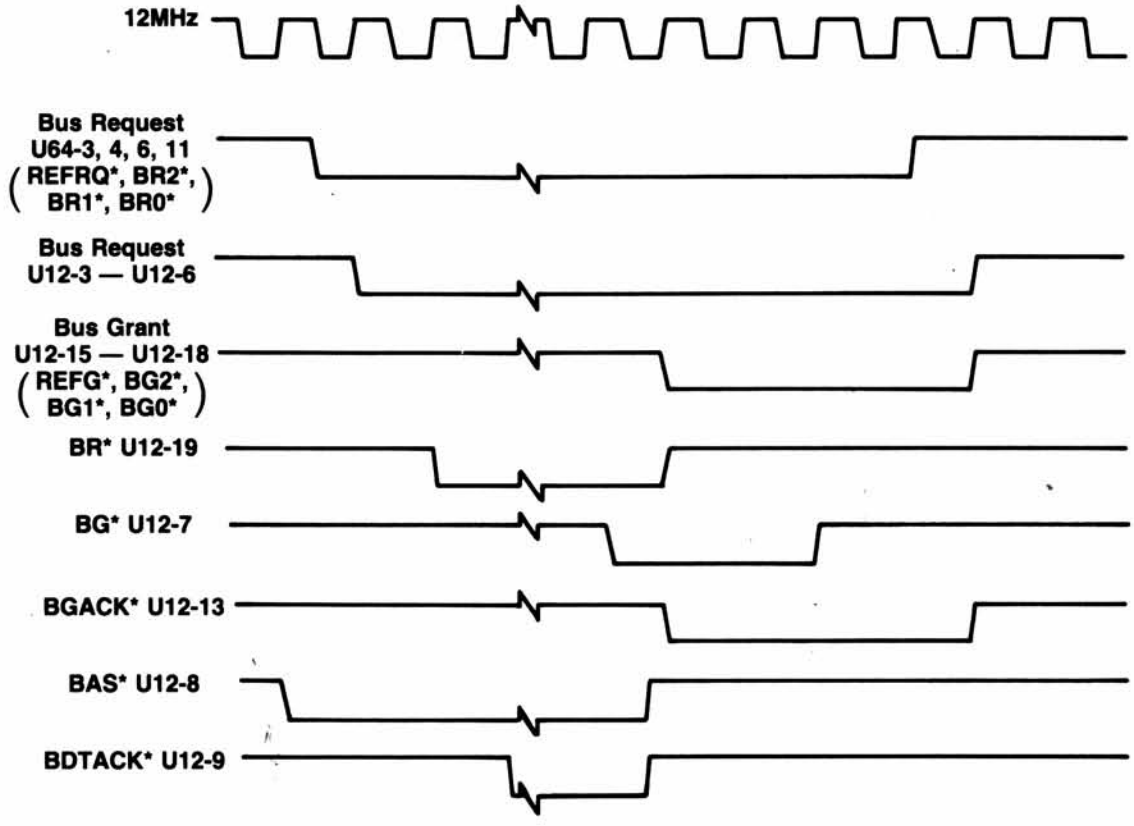


Figure 1. Bus Arbitration Circuit Timing

Section 6.Ø Data Transfer Acknowledge Logic

Data Transfer Acknowledge (DTACK*) is the asynchronous handshake signal used by memory and peripheral devices to complete a bus cycle. When BDTACK* is asserted during a

read bus cycle, the data is latched into the 68ØØØ CPU and the bus cycle is terminated. Assertion of BDTACK* during a write cycle causes the 68ØØØ CPU to terminate the bus cycle.

There are two main sources of BDTACK* from the CPU's point of view:

- Onboard devices, such as the AM9519 interrupt controller chip and the memory management registers.
- Offboard devices, such as memory or peripherals connected to the 68ØØØ bus.

Two signals can trigger the generation of an onboard BDTACK* -- MIIDTACK* and RIP*.

If MIIDTACK* is asserted, a read or write to an onboard device is in progress.

If RIP* is asserted, an interrupt acknowledge cycle is in progress and the interrupt vector data is valid from the interrupt controller chip U11.

MIIDTACK* and RIP* are OR'ed together at U3Ø pin 12 and U3Ø pin 13, and the resultant output at U3Ø pin 11 clocks a low into the D flip-flop (1/2 of U48). This results in a high output at U48 pin 6, which is inverted by 1/6 of U5Ø and used to drive the BDTACK* line low.

Address Strobe (AS) sets the flip-flop and negates BDTACK* for the next bus cycle. **Figure 2** shows the timing relationships for onboard BDTACK* generation.

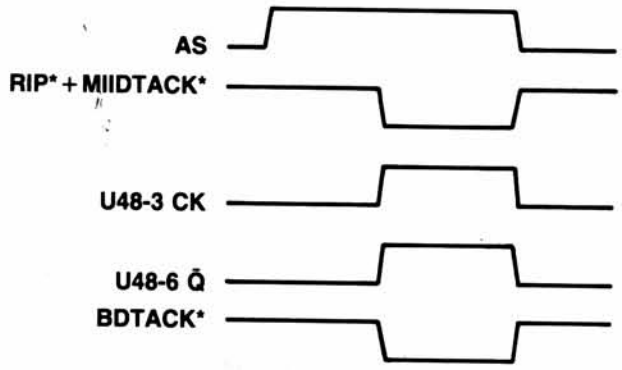


Figure 2. Onboard BDTACK Generation

Generation of BDTACK* from offboard devices is only from the 68ØØØ memory boards. BDTACK* being asserted from a 68ØØØ memory board indicates that data transfer has been completed.

During a read cycle, BDTACK* indicates that the data from the data bus has been written into memory and has completed the transfer. During a write cycle, BDTACK* indicates that the data requested is present on the data bus. For more details on memory BDTACK* generation, refer to the Theory of Operation for the Model 16 Memory Board.

BDTACK* is also generated for the time-out error logic located in the middle and bottom of sheet 2 of the 68ØØØ CPU schematic. BDTACK* is driven by 1/6 of U5Ø and is generated by the Q output of U62 pin 9.

The Q output of U62 pin 9 (TMERR) indicates that a non-responding device has been accessed and a time-out error has occurred.

Section 7.Ø 68ØØØ I/O Decoding and Strobes

The I/O devices in the 68ØØØ subsystem are memory-mapped and consist of the:

- Interrupt controller chip.
- Memory management registers.
- Z8Ø interrupt (NOT implemented in Model II upgrades).

All other I/O devices and peripherals in the Model 16 are still controlled by the Z8Ø CPU.

The main I/O decoding is managed by two chips (U49 and U57) which make up the I/O controller. The I/O controller interfaces the 68ØØØ CPU to the 68ØØØ subsystem I/O devices, thereby providing all necessary signals.

The middle and top of sheet 2 of the 68ØØØ CPU schematic should be referenced unless otherwise noted. The current I/O devices are mapped at address locations 78ØØDØH to 78ØØD7H. Address bits KA2Ø-KA22 are decoded by a 3 input and gate, 1/3 of U4, which generates the signal VMIIAD.

VMIIAD and mIO (KA19) are connected to the I/O controller and generate the I/O signals during access to memory space

78ØØØØH to 78FFFFH. When an I/O access is executed, VMIIAD, mIO, AS*, and the 8-MHz CK (clock) start a 4-bit internal counter to U49. This counter strobes the assertion of BIORQ*, BRD*, and BWR* of U49 and MIIDTACK* of U57.

SRW* (R/W*) determines the assertion of BRD* or BWR*. BIORQ* is used to enable a 1 of 8 decoder U32 which decodes address bits KA1-KA7. Refer to the bottom right-hand corner of sheet 3 of the 68ØØØ CPU schematic.

KA4, KA6, and KA7 are decoded by a 3 input and gate, 1/3 of U27, and the output is connected to the active-high enable input U36 pin 6. KA5 enables the third enable input U36 pin 4 when an active low occurs.

KA1-KA3 are decoded to determine the output of U32 that selects the I/O device. **Table 2** outlines the memory-mapped I/O locations currently implemented in the 68ØØØ subsystem. See **Figure 3** for the timing relationships of the I/O controller (U49 and U57).

Address	Function
78ØØDØ	Interrupt controller data register
78ØØD1	Interrupt controller command register
78ØØD2	Limit register two
78ØØD3	Offset register two
78ØØD4	Limit register one
78ØØD5	Offset register one
78ØØD6	Interrupt request to Z8Ø
78ØØD7	Interrupt request to Z8Ø

Table 2. Memory-Mapped I/O Locations

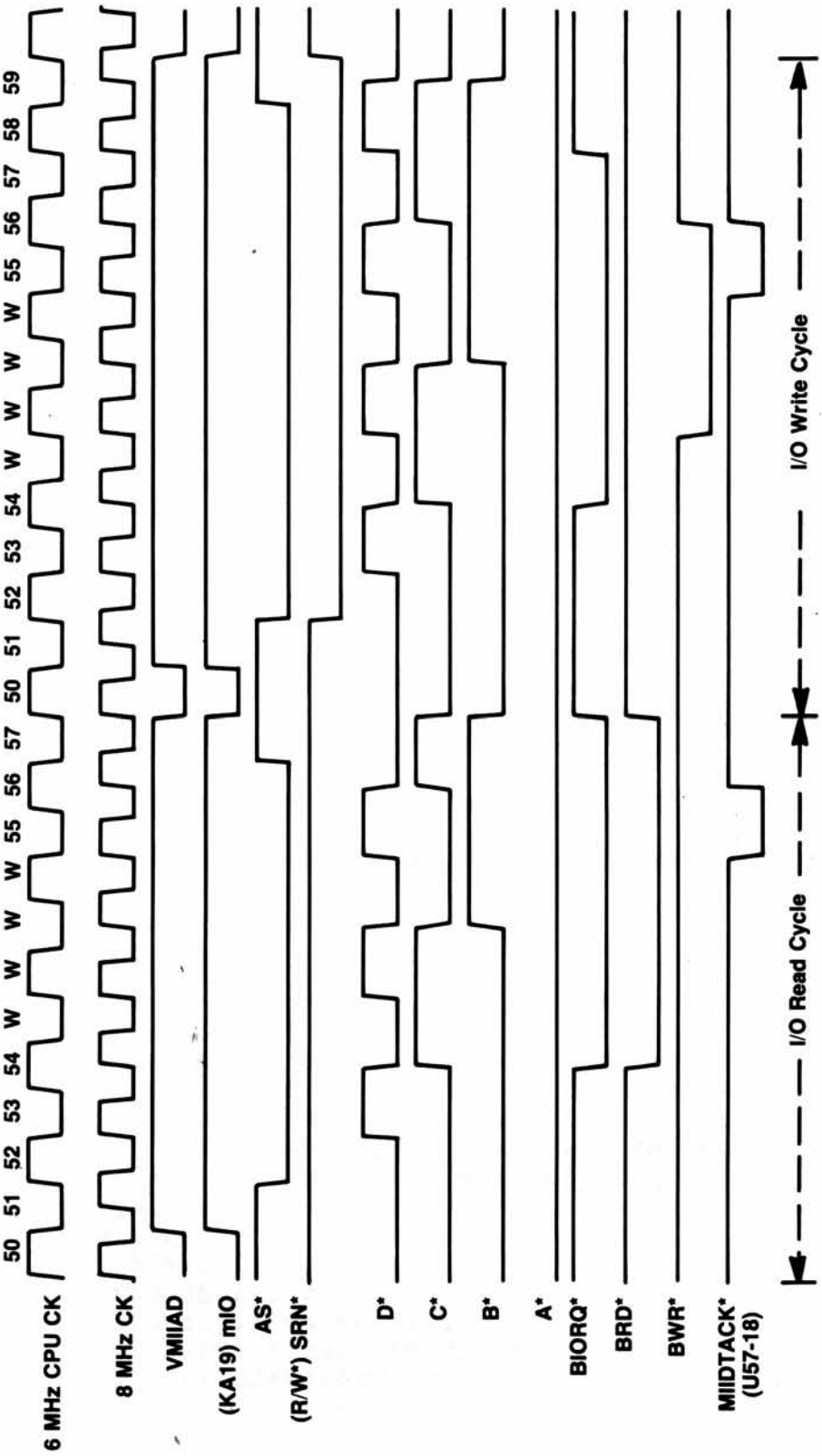


Figure 3. I/O Controller Timing

Table 3 outlines the memory map of the 68ØØØ subsytem:

SYSTEM RAM

Start Address	End Address	Total Bytes
Total Available RAM Space		
ØØØØØØ	6FFFFF	7 MEG
One 128K Memory Board Installed		
ØØØØØØ	Ø1FFFF	128K
Two 128K (or One 256K) Memory Boards Installed		
ØØØØØØ	Ø3FFFF	256K
One 256K and One 128K Memory Board Installed		
ØØØØØØ	Ø5FFFF	384K
Two 256K Memory Boards Installed		
ØØØØØØ	Ø7FFFF	512K

Table 3. Memory Map of the 68ØØØ Subsystem

Section 8.Ø Clock Logic

The clock logic provides the clocks and timing for the 68ØØØ subsystem. The heart of the clock logic is a 24-MHz crystal oscillator. (See the top left-hand corner of sheet 2 of the 68ØØØ CPU schematic.) The output of the 24-MHz oscillator is hooked to U63 pin 4 (74S86) which stabilizes the voltage levels. The output of U63 pin 6 is divided by two by 1/2 of U47 (74LS74) which provides the 12-MHz clock. The 12-MHz clock is divided by two by 1/2 of U47 (74LS74) to provide the 6-MHz clock or PCLOCK. The 24-MHz clock at U63 pin 6 is also sent to a logic circuit consisting of U55 (74S112), 1/4 of U63 (74S86), 1/4 of U38 (74LS32), and 2/3 of U27 (74LS11). This circuit causes division by 1.5 that outputs a non-symmetrical 16-MHz signal at U38 pin 3. The 16-MHz signal is divided by two by 1/2 of U54 (74LS74) which

provides the 8-MHz clock. The 8-MHz clock is also divided by two by 1/2 of U54 (74LS74) to provide the 4-MHz clock.

Section 9.Ø Refresh Logic

The refresh logic provides the necessary timing and control for generating the refresh pulses required for the dynamic RAMs on the 68ØØØ memory board(s). It provides refresh by becoming bus master and supplying the refresh strobe REFRSH. The timing is generated by a LS393 counter (U45) and decoding steering logic LS32 (U38) and LS3Ø (U53).

The timing logic generates a bus request (REFRQ*) every 15.5 or 31 usec, depending on the configuration of the jumper on E43, E44, and E45. If E44 and E45 are jumped, U53 will trigger the D flip-flop 1/2 U62 on the count of 62 which equals 15.5 usec. This will meet the minimum requirement of 128 refreshes every 2 msec. If E43 and E44 are jumped, the D flip-flop will be triggered on the count of 124 which will equal 31 usec. This configuration will generate less refresh bus request cycles, thus allowing more CPU running time; but to meet the 2-msec refresh specification, two refresh pulses are generated during each refresh period.

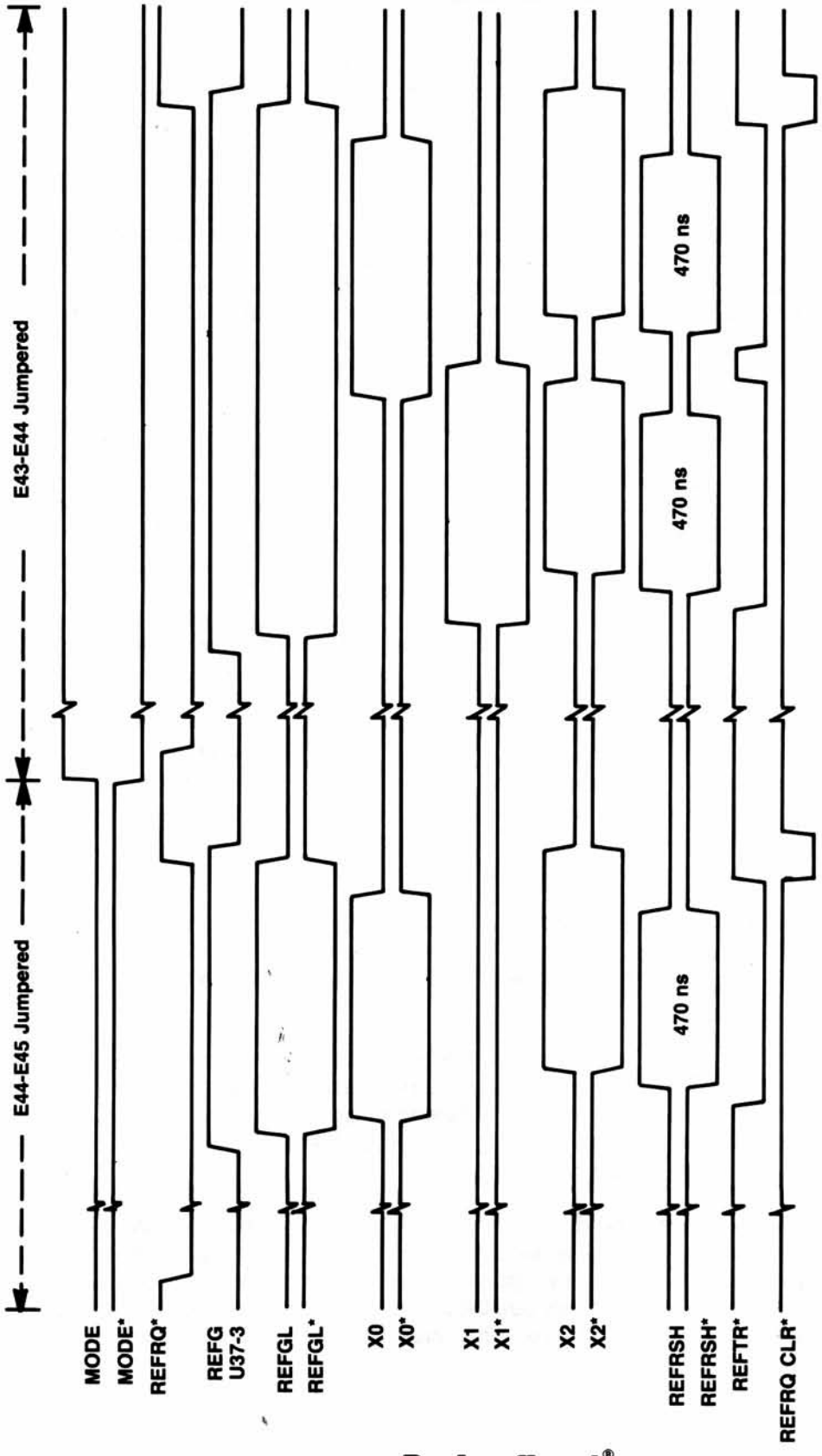
The generation of the single or double refresh pulse is the function of a refresh state machine consisting of three S64's (U2Ø, U25, and U26) and a L551 (U19). **Figure 4** shows the timing relationships of the refresh logic.

Section 1Ø.Ø Bus Error Logic

Bus error logic is driven low when one of three events occur:

- An attempt by the user to access memory outside the extents defined by the memory management registers.
- A time-out error on a 68ØØØ memory access.
- A time-out error on a memory access by an external bus master, i.e., the Z8Ø CPU or DMA.

The bus error signal also drives the MEMDIS* bus signal which instructs the 16-bit memory board to abort a memory cycle. This provides a write-protect feature for accesses outside the user's defined extents. A 1ØØ-usec one-shot (1/2 of U39) is used to define the maximum time allowed for a memory cycle.



Note: Each block between signals equals one propagation delay.

Figure 4. Timing for Refresh Logic

The bus Address Strobe (AS*) is used to trigger the one-shot. The active-low output of the one-shot is the clock input to a D flip-flop (1/2 of U62). If the one-shot ever times-out, the rising edge of the active-low output will clock the state of BDTACK* into the D flip-flop.

The Q output of the flip-flop is inverted by an open collector device and drives the BDTACK* line. If BDTACK* is high, indicating that the memory or I/O device did not respond, then BDTACK* is driven low which allows the cycle to complete. TMERR* is also driven by the Q output of the flip-flop. Thus, if a device on the bus fails to respond within the timespan allotted by the time-out circuit, a bus error will be generated.

Model 16 Memory Board Theory of Operation

The Model 16 Memory Board is a Random Access Memory (RAM) with a total capacity of 128K words (256K bytes) of data with optional byte parity for error detection. It is designed for use with the 68ØØØ processor system. The 68ØØØ has a 16-bit-wide data bus and, therefore, the memory is 16 bits wide.

Because the MC68ØØØ needs to handle both 8- and 16-bit-wide data transactions, the memory is further divided into upper and lower bytes (8). Actually, all transfers to and from memory are treated as byte transfers. If a full 16-bit transfer is desired, an upper and lower byte transaction is performed simultaneously. Thus, the memory is organized as two parallel byte memories which share a common memory space.

Since parity is checked on all transfers, if the option is enabled, the parity generating/checking has to be set up on a byte basis; therefore, each byte has a ninth bit added called a parity bit. Parity is a scheme where the total number of bits that = 1 in every valid memory location is either EVEN or ODD. The Model 16 memory uses the odd scheme. Thus, if the data has an even number of bits = 1 (Ø,2,4,6,or 8), the parity bit will = 1, making the total number of bits = 1 odd. Otherwise, the parity bit = Ø.

Functional Description

The Model 16 Memory Board can functionally be divided into four main parts:

- Address circuits.
- Timing circuits.
- Parity circuits.
- Memory.

Memory

By understanding the requirements of the memory IC's, the address and timing circuits are clearer. The basic memory element is a DRAM (Dynamic Random Access Memory) IC containing 65,536 (64K) single-bit locations. Therefore, to store each byte with parity, nine IC's are required.

Two particulars of dynamic RAM's are address multiplexing and refresh. There are 16 address lines to access this amount of memory. Address line AØ, internal to the 68ØØØ CPU, is used to distinguish between upper (AØ=1) and lower (AØ=Ø) bytes; then A1-A16 is required. To save pins and chip size, the IC's have only 8 address inputs.

Therefore, the address lines are loaded into memory in two parts:

- Row address (A1-A8), first by the Row Address Strobe (RAS).
- Column address (A9-A16), second by the Column Address Strobe (CAS).

Once the addresses are loaded, the memory alters or presents the data at that location, depending on the state of the Read/Write (R/W*) signal. Refresh is required to maintain the information stored in the RAMs.

Every 2 milliseconds, the entire contents of the RAM must be rewritten. Due to the RAM structure, this requires 128 refresh-only accesses every 2.Ø ms, or one every 16.Ø microseconds. The refresh cycle is the same as a read cycle, except AMUX and CAS are not generated.

Address

Address lines BA1* through BA16* are routed to the board through two-line receiver-inverting buffers U3,U4 (74S24Ø) which are permanently enabled. The lower eight address lines (BA1-BA8) are multiplexed by U28,U48, with the eight refresh address bits from the refresh address counter U14 becoming the eight memory row address bits.

The row address bits are then multiplexed by U29,U49, with the column address bits (address lines BA9-BA16) becoming the eight multiplexed memory address bits. The memory address lines are routed to all 36 IC's through series resistors to reduce ringing and overshoot.

Address line BA17* is routed to the memory board by non-inverting buffer U9. A17 enables the steering AND gates to generate the RAS signals for the lower or upper 128K memory page. Address lines BA18-BA22 are used to enable the memory board at a specific 256K location within the 68ØØØ subsystem memory map allocation.

These address lines are connected to an 8-bit magnitude comparitor U2 (LS688) which compares two 8-bit inputs. The address lines are compared to a preset value by the use of dip switch S1. If the address lines BA18-BA22 equal the preset value, the output of the comparitor is asserted and enables the memory board. Refer to **Table 4** for proper setting of S1.

Control/Timing

The control and timing signals consist of Bus Address Strobe (BAS*), Bus Upper Data Strobe (BUDS*), Bus Lower Data Strobe (BLDS*), Bus Read/Write (BR/W*), Memory Disable (MEMDIS*, which is BERR*), and Bus Data Transfer Acknowledge (BDTACK*).

All signals, except BDTACK*, are input signals from the 68ØØØ CPU board and are interfaced to the memory board through U9 (S241). BDTACK* is an output control signal to the 68ØØØ CPU board and is driven by an open collector NAND gate U1 pin 3 (7438).

The output of U1Ø pin 8 (UDSG) represents the logical AND of AS*, UDS*, board select from U2 pin 19, and MEMDIS. U1Ø pin 6 (LDSG) represents either the logical AND of AS*, LDS*, BDSEL*, and MEMDIS OR REF* (refresh). These two outputs are

	S1							
			(B18)		(B19)	(B22)	(B20)	(B21)
	1	2	3	4	5	6	7	8
Disable Board	X	Ø	X	X	X	X	X	X
ØØØØØØ-Ø3FFFF	X	1	Ø	X	Ø	Ø	Ø	Ø
Ø4ØØØØ-Ø7FFFF	X	1	1	X	Ø	Ø	Ø	Ø
Ø8ØØØØ-ØBFFFF	X	1	Ø	X	1	Ø	Ø	Ø
ØCØØØØ-ØFFFFF	X	1	1	X	1	Ø	Ø	Ø
1ØØØØØ-13FFFF	X	1	Ø	X	Ø	Ø	1	Ø
14ØØØØ-17FFFF	X	1	1	X	Ø	Ø	1	Ø
18ØØØØ-1BFFFF	X	1	Ø	X	1	Ø	1	Ø
1CØØØØ-1FFFFF	X	1	1	X	1	Ø	1	Ø
2ØØØØØ-23FFFF	X	1	Ø	X	Ø	Ø	Ø	1
24ØØØØ-27FFFF	X	1	1	X	Ø	Ø	Ø	1
28ØØØØ-2BFFFF	X	1	Ø	X	1	Ø	Ø	1
2CØØØØ-2FFFFF	X	1	1	X	1	Ø	Ø	1
3ØØØØØ-33FFFF	X	1	Ø	X	Ø	Ø	1	1
34ØØØØ-37FFFF	X	1	1	X	Ø	Ø	1	1
38ØØØØ-3BFFFF	X	1	Ø	X	1	Ø	1	1
3CØØØØ-3FFFFF	X	1	1	X	1	Ø	1	1
4ØØØØØ-43FFFF	X	1	Ø	X	Ø	1	Ø	Ø
44ØØØØ-47FFFF	X	1	1	X	Ø	1	Ø	Ø
48ØØØØ-4BFFFF	X	1	Ø	X	1	1	Ø	Ø
4CØØØØ-4FFFFF	X	1	1	X	1	1	Ø	Ø
5ØØØØØ-53FFFF	X	1	Ø	X	Ø	1	1	Ø
54ØØØØ-57FFFF	X	1	1	X	Ø	1	1	Ø
58ØØØØ-5BFFFF	X	1	Ø	X	1	1	1	Ø
5CØØØØ-5FFFFF	X	1	1	X	1	1	1	Ø
6ØØØØØ-63FFFF	X	1	Ø	X	Ø	1	Ø	1
64ØØØØ-67FFFF	X	1	1	X	Ø	1	Ø	1
68ØØØØ-6BFFFF	X	1	Ø	X	1	1	Ø	1
6CØØØØ-6FFFFF	X	1	1	X	1	1	Ø	1

Ø = Off = Open
1 = On = Closed
X = Don't Care

Table 4. Memory Map Select Table

OR'ed together by U11 so either or both will initiate a memory request cycle.

The output of U11 pin 8 (MEMREQ) clocks the D flip-flop (1/2 of U12) to start a pulse down a delay line U13. The pulse output at the 40-ns tap is RAS, at 80 ns is AMUX, at 120 ns is CAS, and at 200 ns is (TERMinate), which clears the flip-flop (U12) and limits the pulse to 200 ns. RAS from the 40-ns output enables the steering logic.

MEMDIS is a signal used by the Memory Management Unit to prevent access to memory, especially writes. In addition to being a term in MEMREQ, it is OR'ed with (TERM) as extra insurance to prevent an access cycle. MEMDIS should be true before UDS*/LDS*. The signal RAS is AND'ed with the four combinations of LDSG, UDSG, A17 and A17* at U24,U25 to make four signals.

These four signals are OR'ed with REF at U23 to generate RAS1L, RAS1U, RAS2L, and RAS2U, a Row Address Strobe for each memory byte section. The signal CAS is AND'ed with (disabled by) REF to generate CASU and CASL, the Column Address Strobe for each word section. The signal R/W* is AND'ed at U15 with UDSG to generate R/W* UPPER BYTE, and with LDSG to generate R/W* LOWER BYTE write strobes.

The drivers for each of the signals RAS1L, RAS1U, RAS2L, RAS2U, CASL, CASU, R/W* LOWER BYTE, and R/W* UPPER BYTE are each passed through a series resistor to reduce ringing and undershoot. The signal DTACK* originates from the D flip-flop U12. The CAS pulse from the delay line sets the signal and is reset at the end of {MEMREQ}. An inverter buffers the signal to the MC68000 processor section.

Parity

There are two parity circuits:

- Input parity generators.
- Output parity checkers.

Since there is byte parity, there is one parity bit for each byte. When data is being written to a memory location, the data is monitored by the input parity generators.

The output of this generator is written into the same memory location as the ninth or parity bit. When a byte is being read from a memory location, all nine bits are monitored by

the output parity checkers (the parity bit is not passed on to the bus). If the parity is correct, the output is a logic 1.

If the parity is incorrect, a logic Ø is strobed into D flip-flop U27 by AMUX. This signal is then routed to the selected system interrupt. The signal is cleared by the next AS*. Parity is an optional feature. The lack of it does not alter the memory operation.

3/ Troubleshooting

Isolating the Trouble

Isolate the trouble to the Model 16 boards by running all current Model II diagnostics to verify the Model II area of the Model 16. If any failures are detected, refer to the Model II Technical Reference Manual. If the Model 16 boards are still suspected as being at fault, remove the Model 16 CPU and memory boards and rerun the Model II diagnostics.

Localizing the Trouble

Localize the trouble to the Model 16 68ØØØ CPU Board or the Model 16 128K/256K Memory Board by following the recommended actions in the troubleshooting chart below:

Run Diagnostics	Condition	Possible Fault	Recommended Action
MOD16 Memory Test (uses Z8Ø to test memory)	Test locked-up	Z8Ø to 68ØØØ interface circuit	Check interface controller U34 and select logic.
		Bus arbitration circuit controller U12	Check latch U64 and bus arbitrator.
		Refresh logic	Check all logic in refresh circuit.

Run Diagnostics	Condition	Possible Fault	Recommended Action
	Bad RAM reported	Bad RAM	Calculate and replace bad RAM ICs.
		Z8Ø to 68ØØØ interface circuit	Check all logic in interface circuit.
		Memory board	Refer to Trouble-shooting the Model 16 Memory Board.
	No errors		Refer to Trouble-Shooting the Model 16 CPU Board.

Troubleshooting the Model 16 68ØØØ CPU Board

Run Diagnostics	Condition	Possible Fault	Recommended Action
MOD16 Interrupt Test	Test locked-up on software interrupt	Interrupt circuit	Check interrupt controller U11,ICs U6, U21, & U13. Check also jumpers E19 to E16 and E3 to E1Ø.
		68ØØØ CPU	Replace 68ØØØ.

Run Diagnostics	Condition	Possible Fault	Recommended Action
		Clock logic	Check clock circuit.
	Test locked-up hardware interrupt	Interrupt circuit	Check interrupt controller U11, and all hardware interrupt inputs into U11.
		68ØØØ CPU	Replace 68ØØØ.
		Clock logic	Check clock circuit.
	Software interrupt received was not interrupt-generated	Interrupt controller	Replace interrupt controller U11.
	Hardware interrupt received was not interrupt-generated	Interrupt circuit	Check for shorts on interrupt input lines.
MOD16 Offset/ Limit Test	OBERROR in user range	Offset/Limit registers	Check output address lines for shorts.
	Protected memory modified	U11,U32, or U16	Check listed ICs.

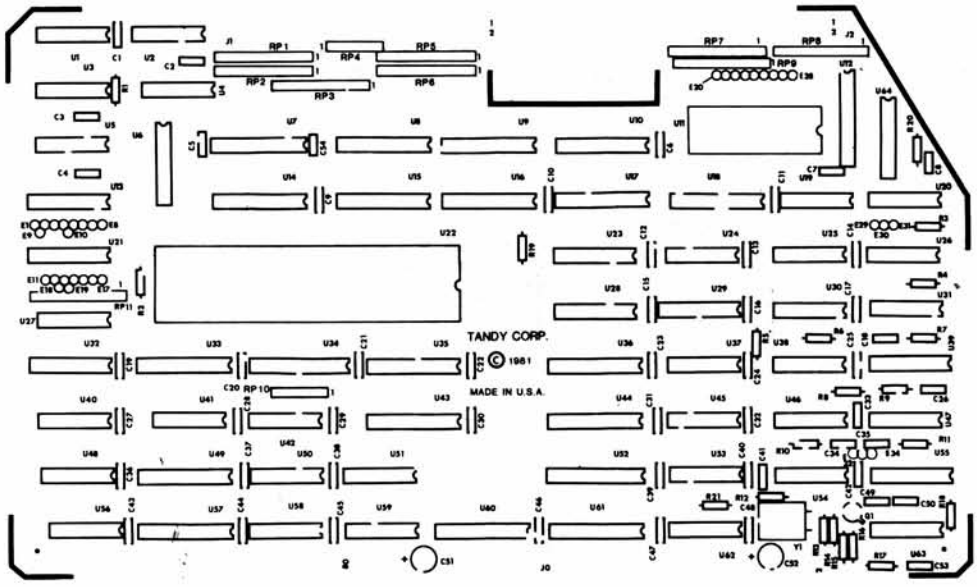
Run Diagnostics	Condition	Possible Fault	Recommended Action
	OBERROR not generated	4-bit full adders	Check U23, U24, U36, or comparitor U41 or U3Ø.
	Random errors	I/O decoding and strobes	Check I/O and strobe circuit.

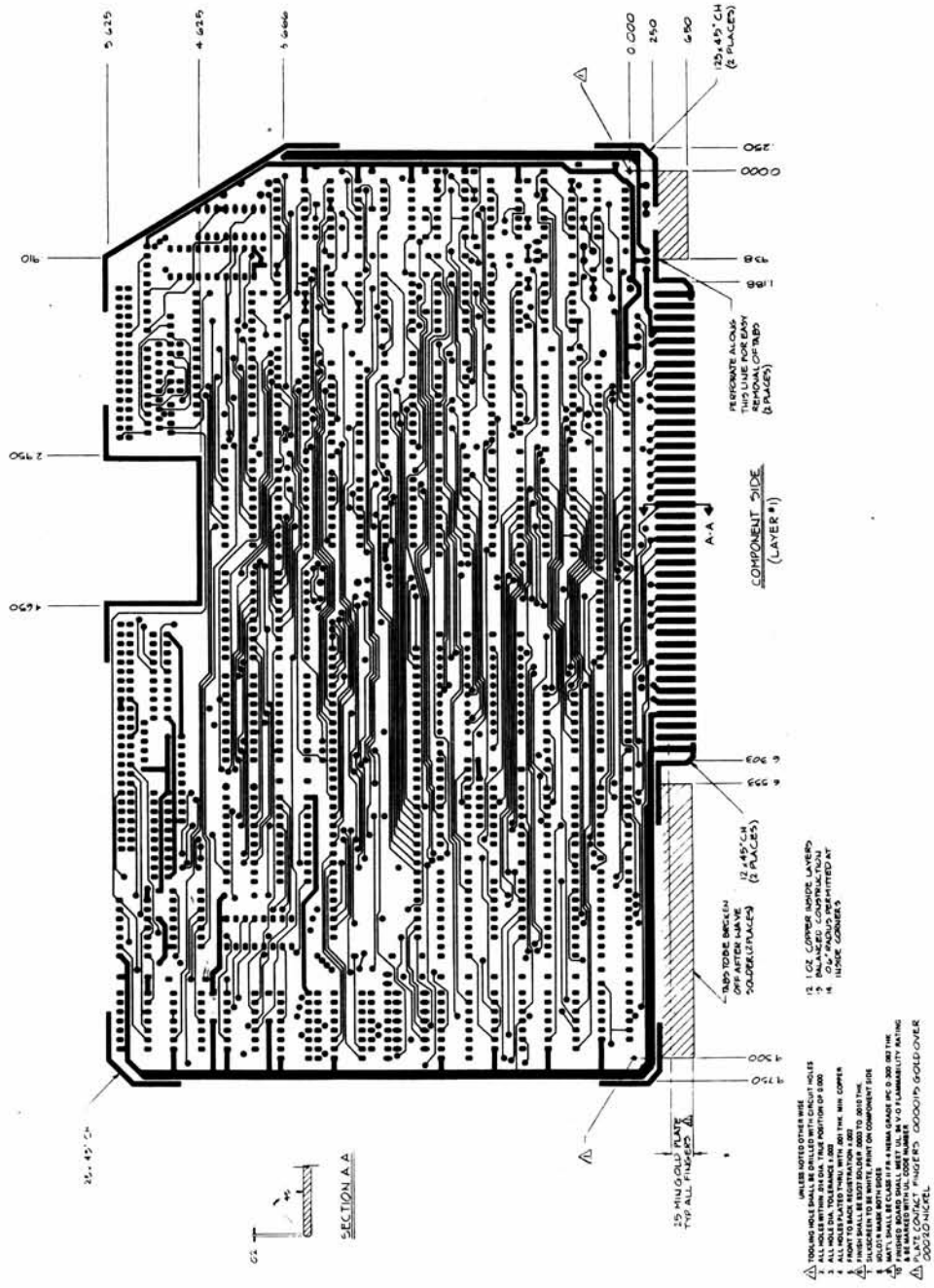
Troubleshooting the Model 16 Memory Board

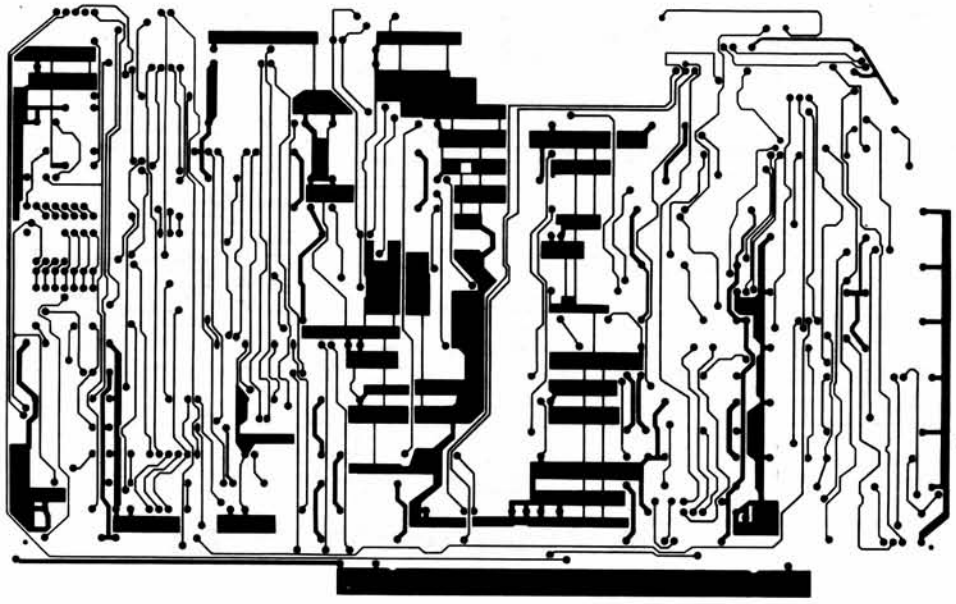
Run Diagnostics	Condition	Possible Fault	Recommended Action
MOD16 Memory Modified Address Test	Bad RAM reported	Bad RAM	Calculate and replace bad RAM IC(s).
		Data buffers	Check buffers U6,U5,U8, and U7.
		Address buffers	Check U4,U3,and U9 for A17.
		Memory control	Check U9 and signal control logic and multi-plexers.

4/ Printed Circuit Boards

68ØØØ CPU Board

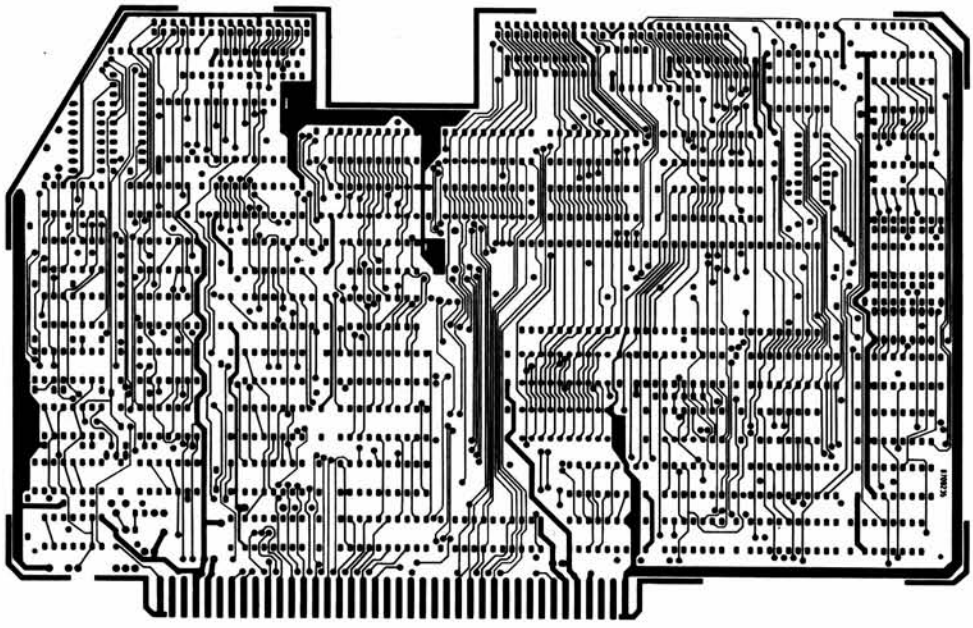



COMPONENT SIDE
(LAYER #1)
SECTION A-A
A-A
TABS TO BE BROKEN OFF AFTER WAVE SOLDERING
.25 MIN GOLD PLATE TYP ALL FINGERS
PLATE CONTACT FINGERS .000015 GOLD OVER .0002 NICKEL



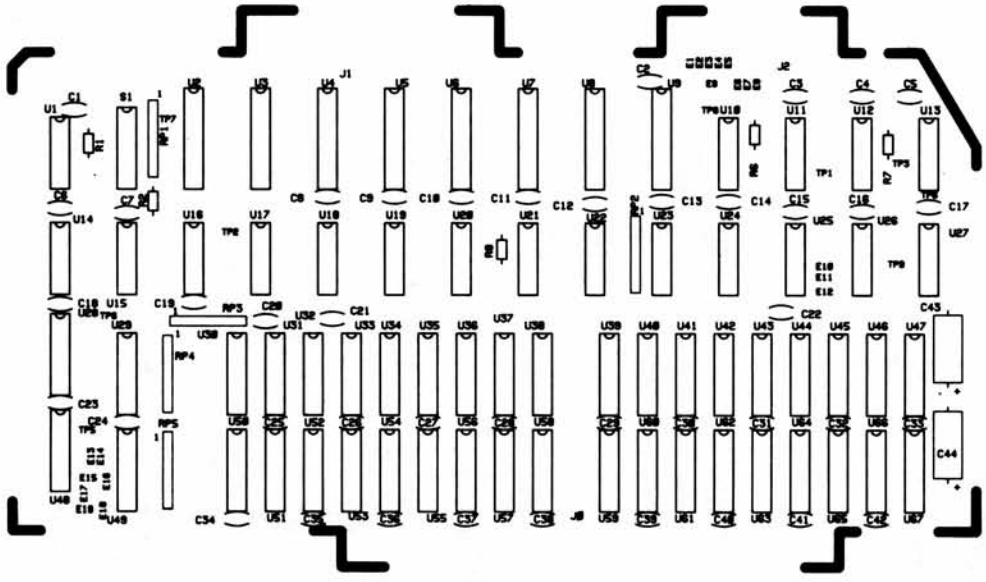
LAYER 2

LAYER 3

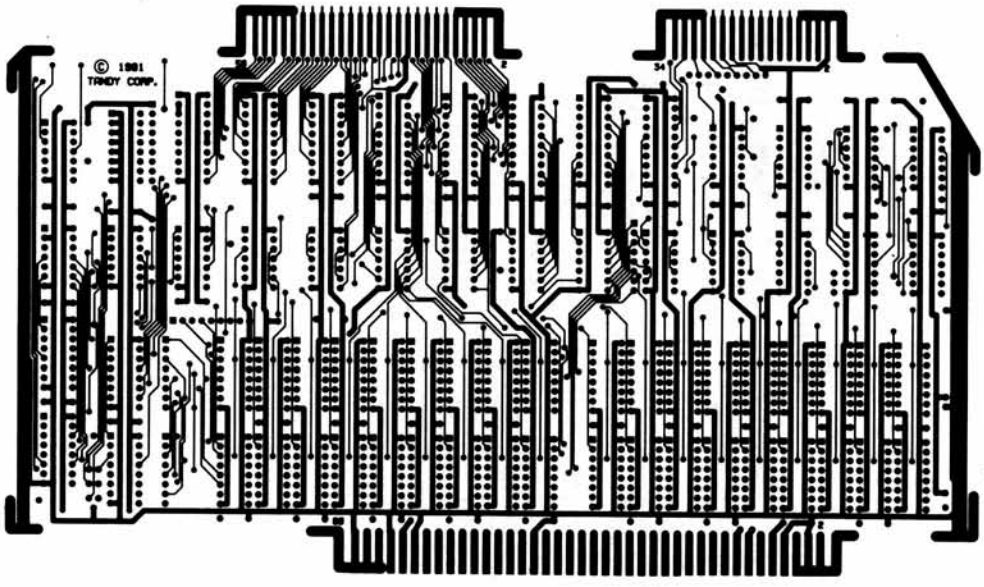


SOLDER SIDE
(LAYER #4)

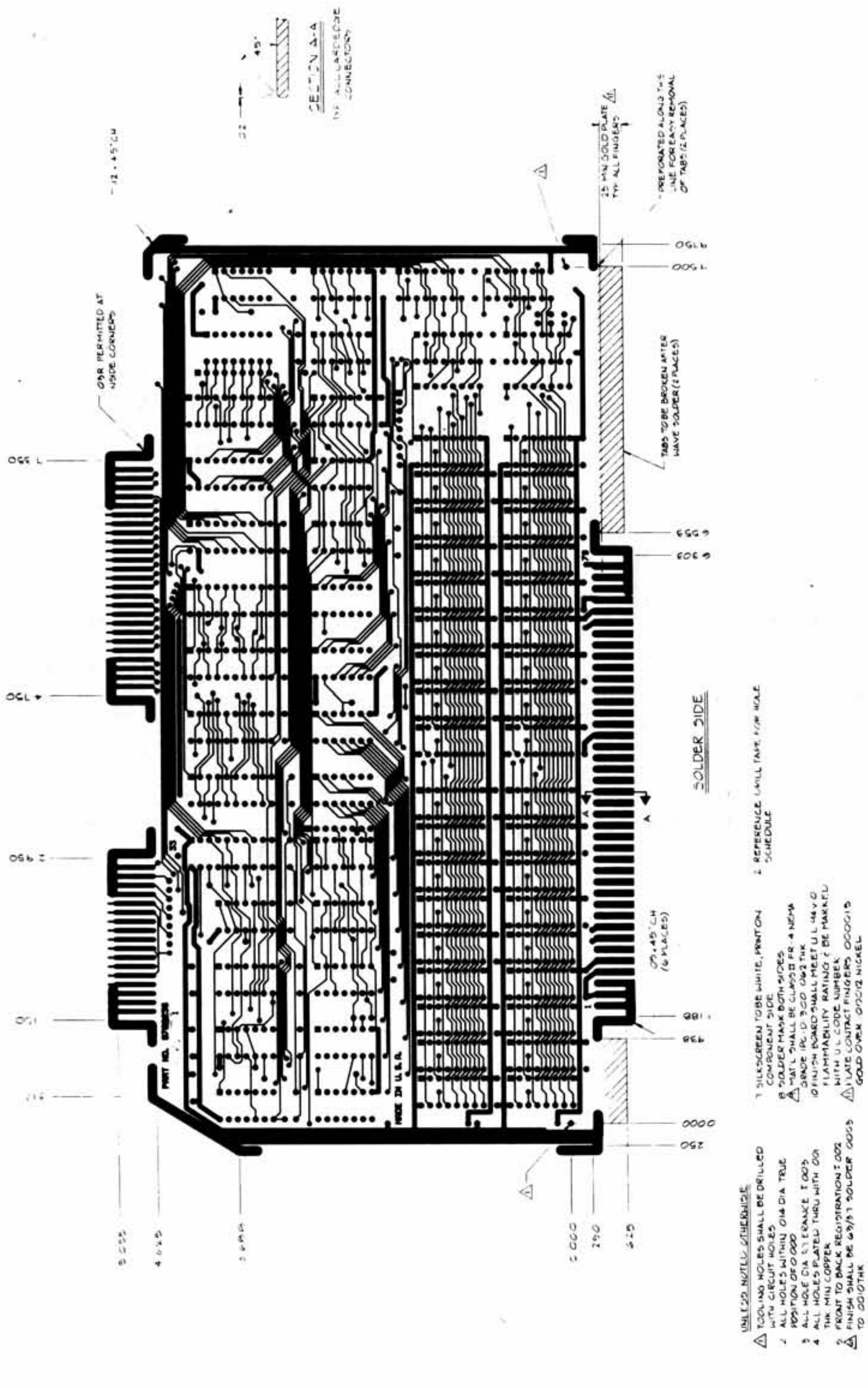
128K/256K Memory Board



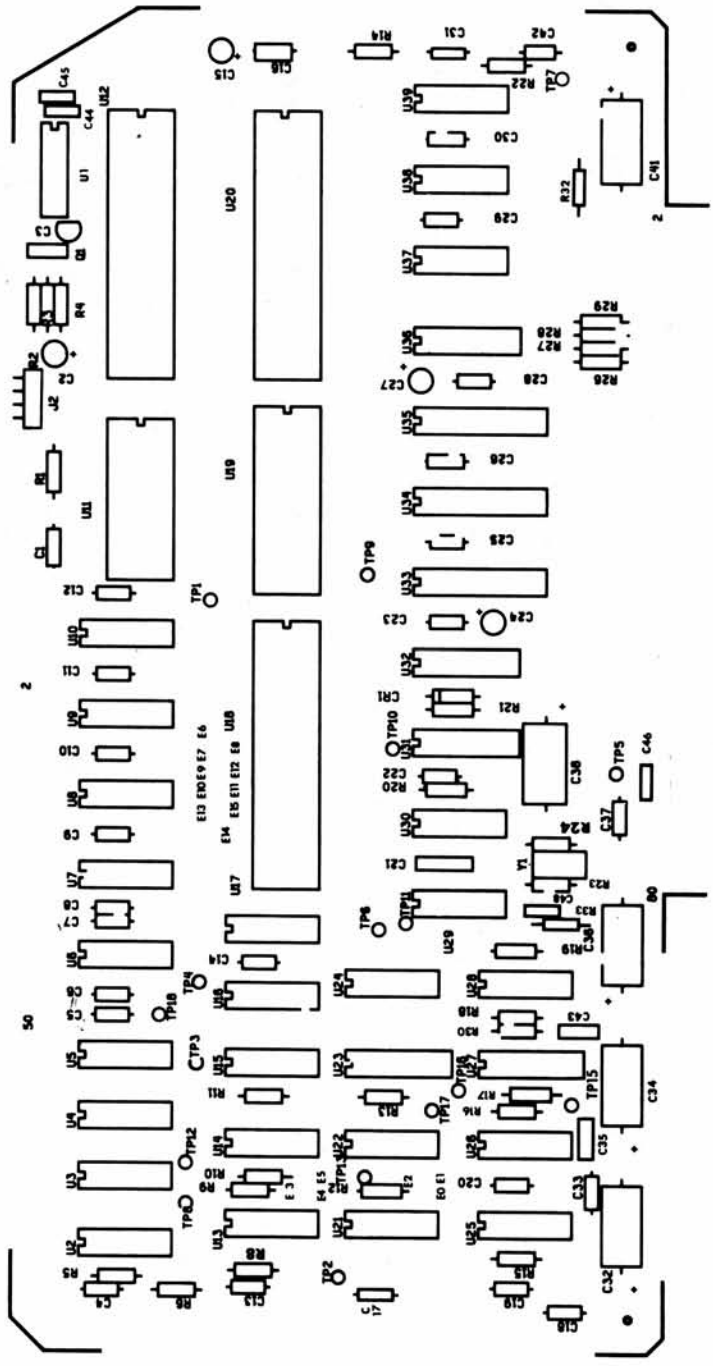
SILKSCREEN

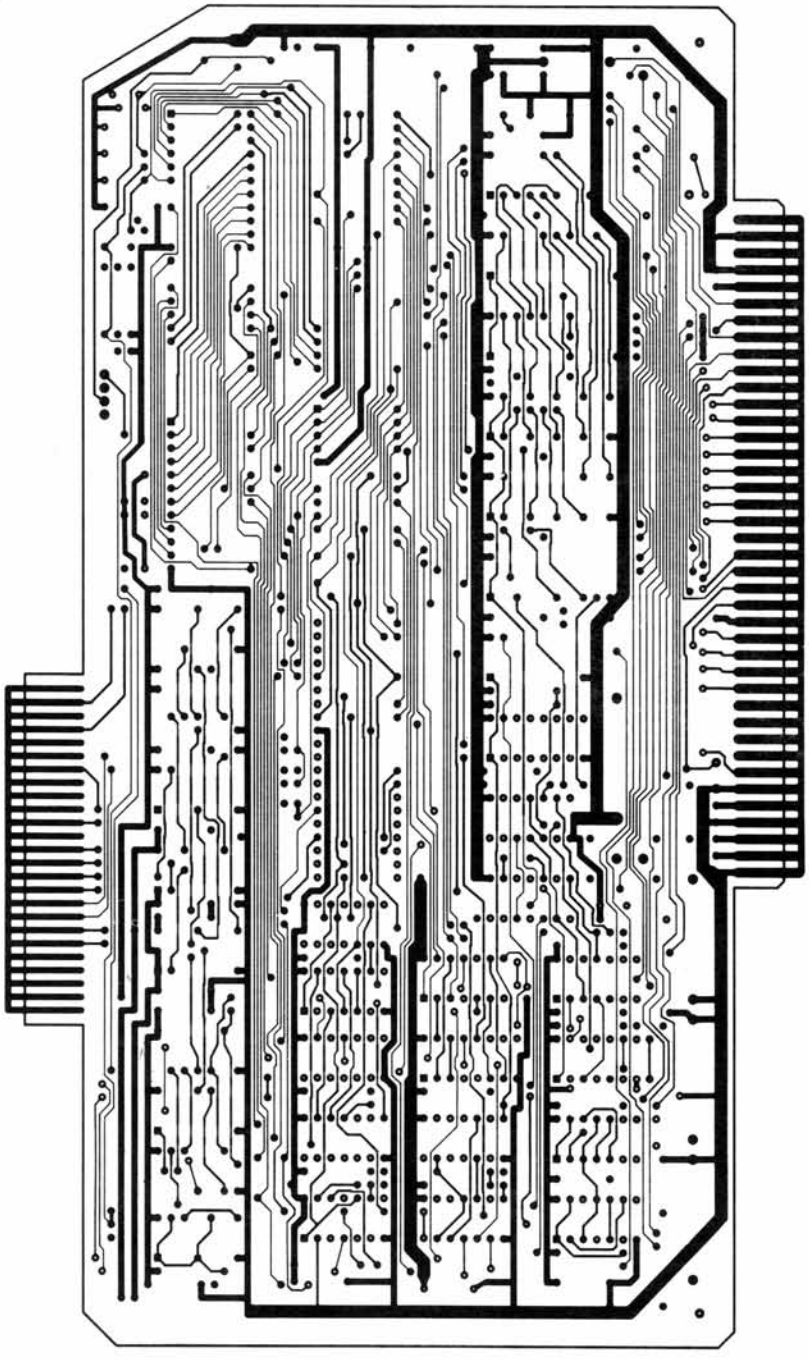


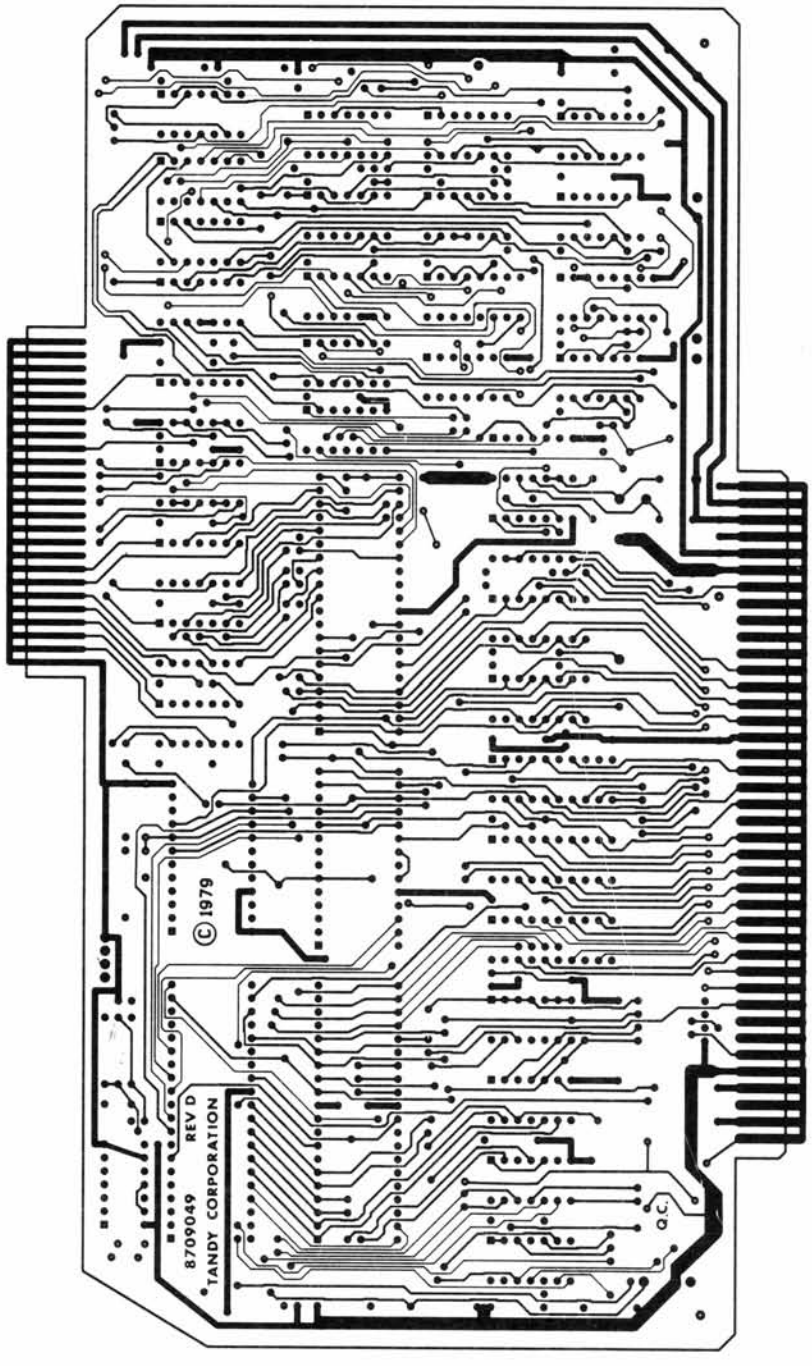
COMPONENT SIDE


SOLDER SIDE

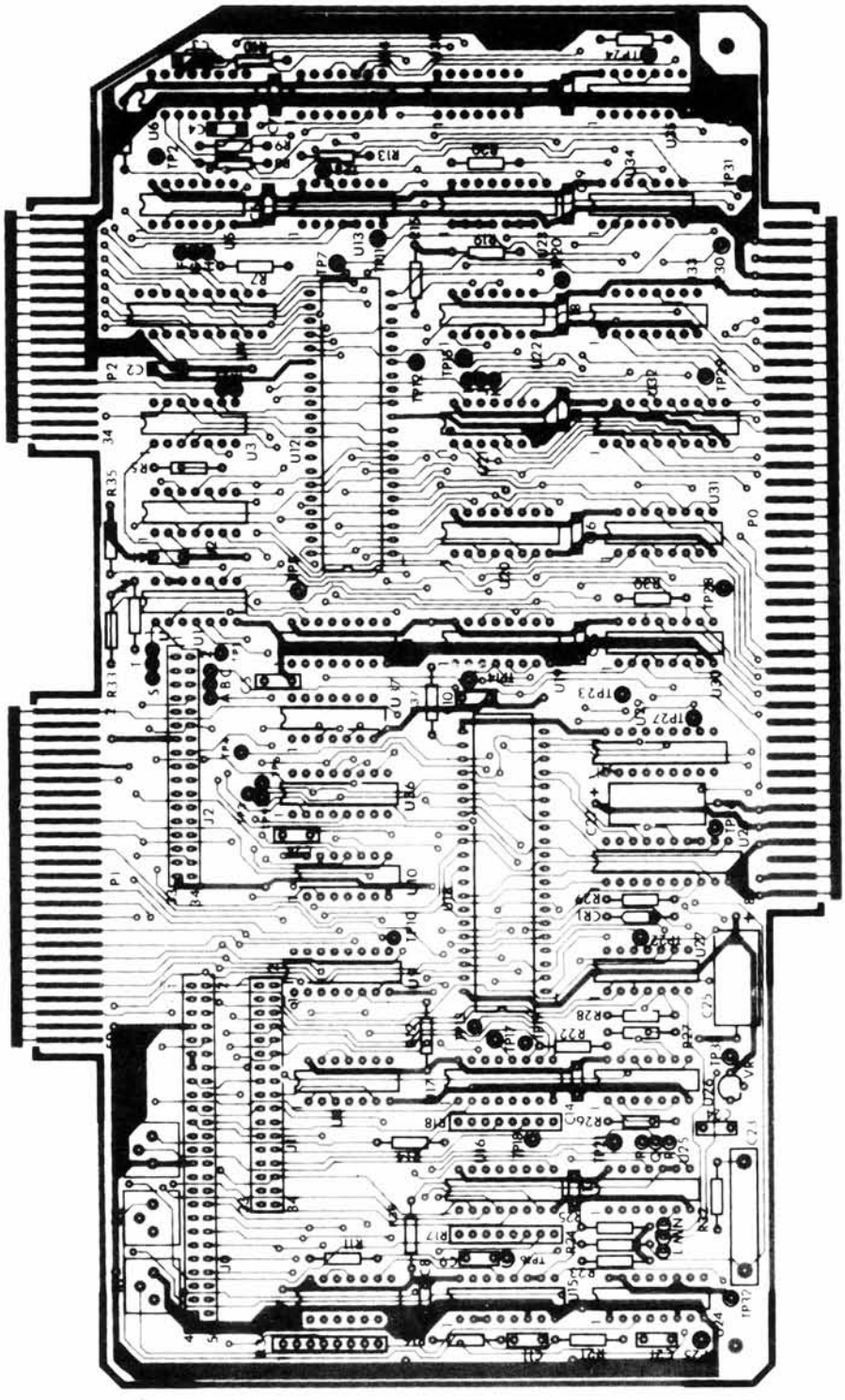
Z8Ø CPU Board

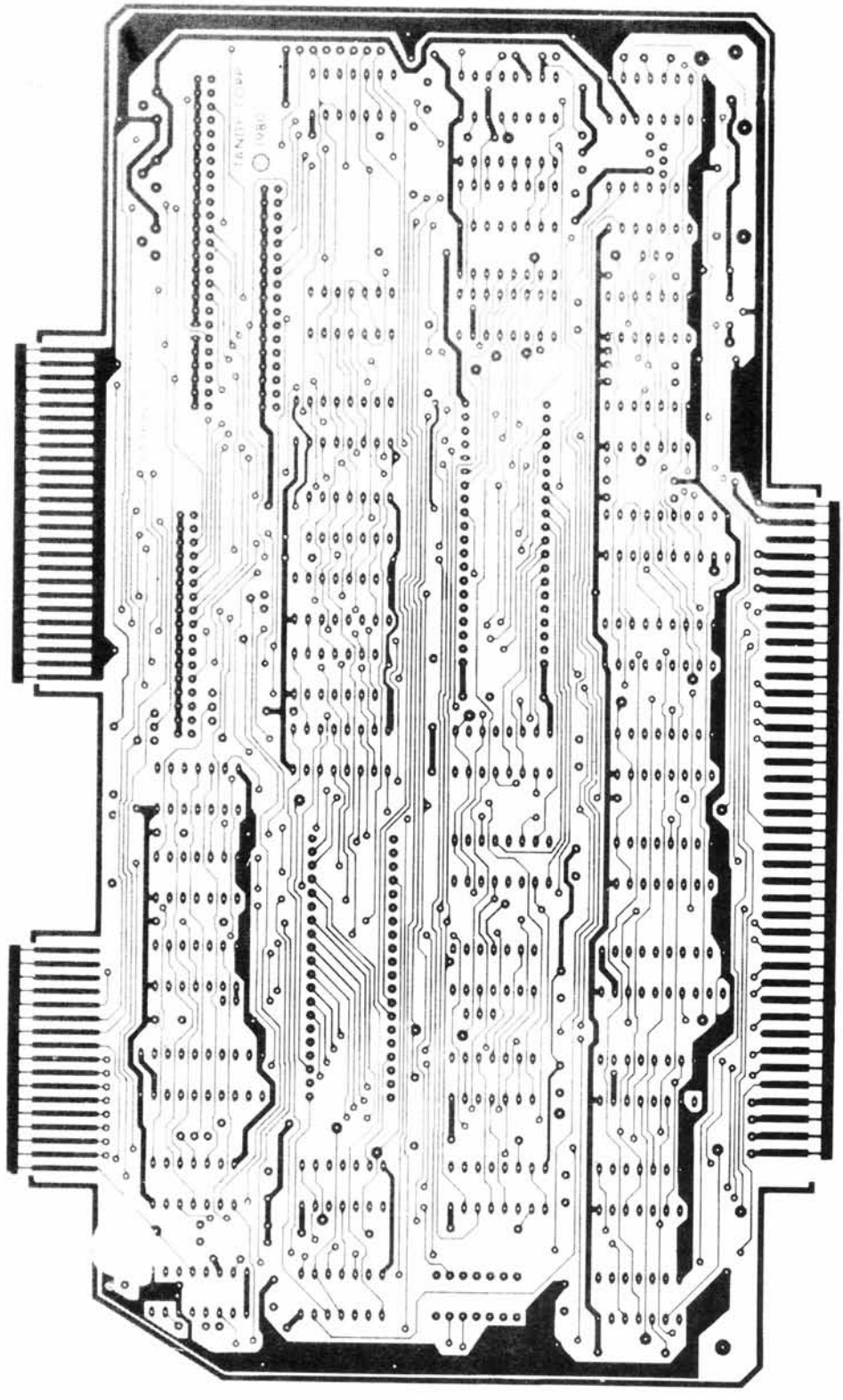




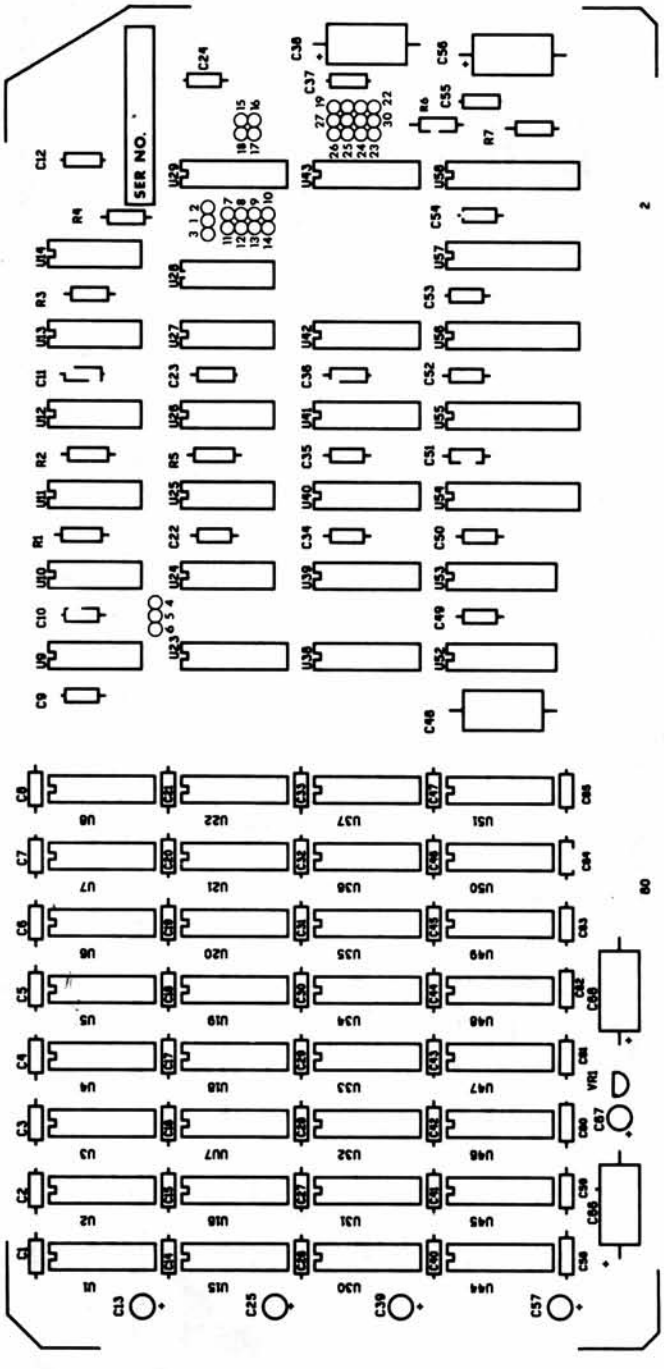

© 1979
8709049 REV D
TANDY CORPORATION
Q.C.

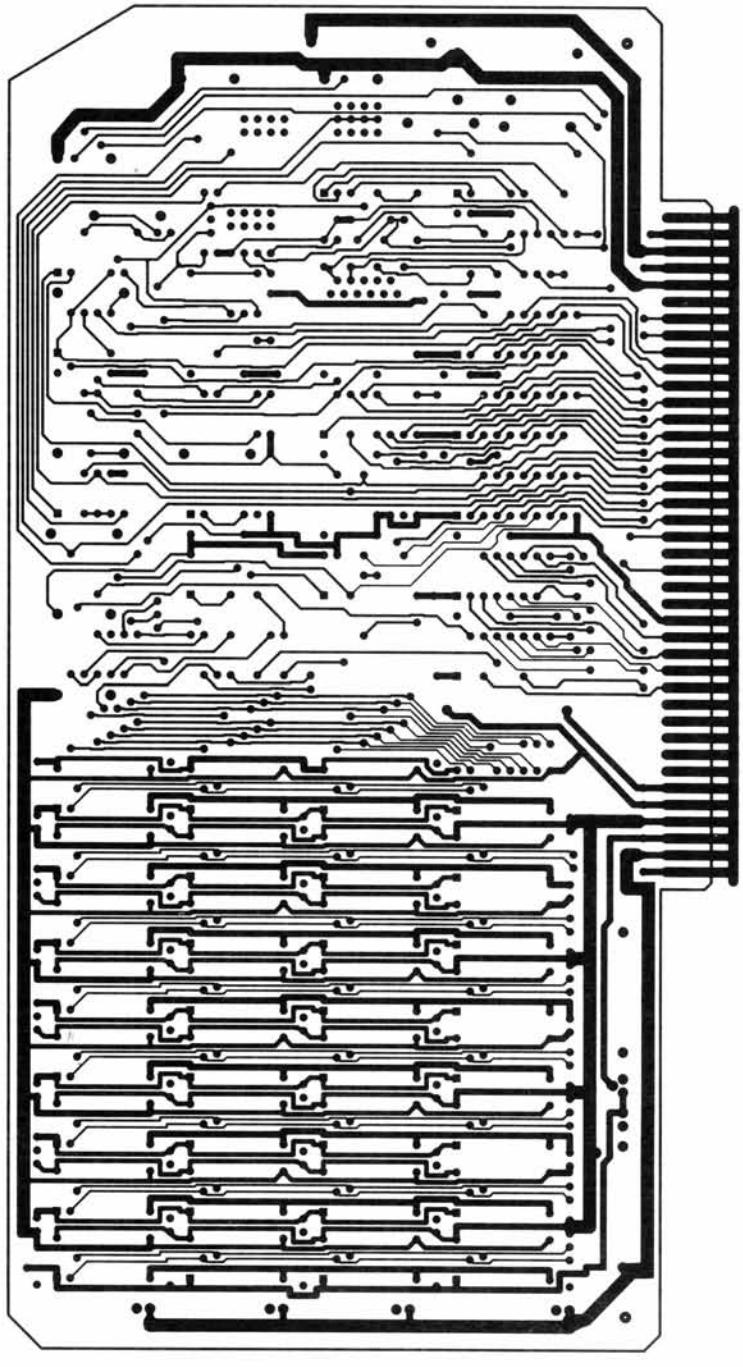
Floppy Disk Board

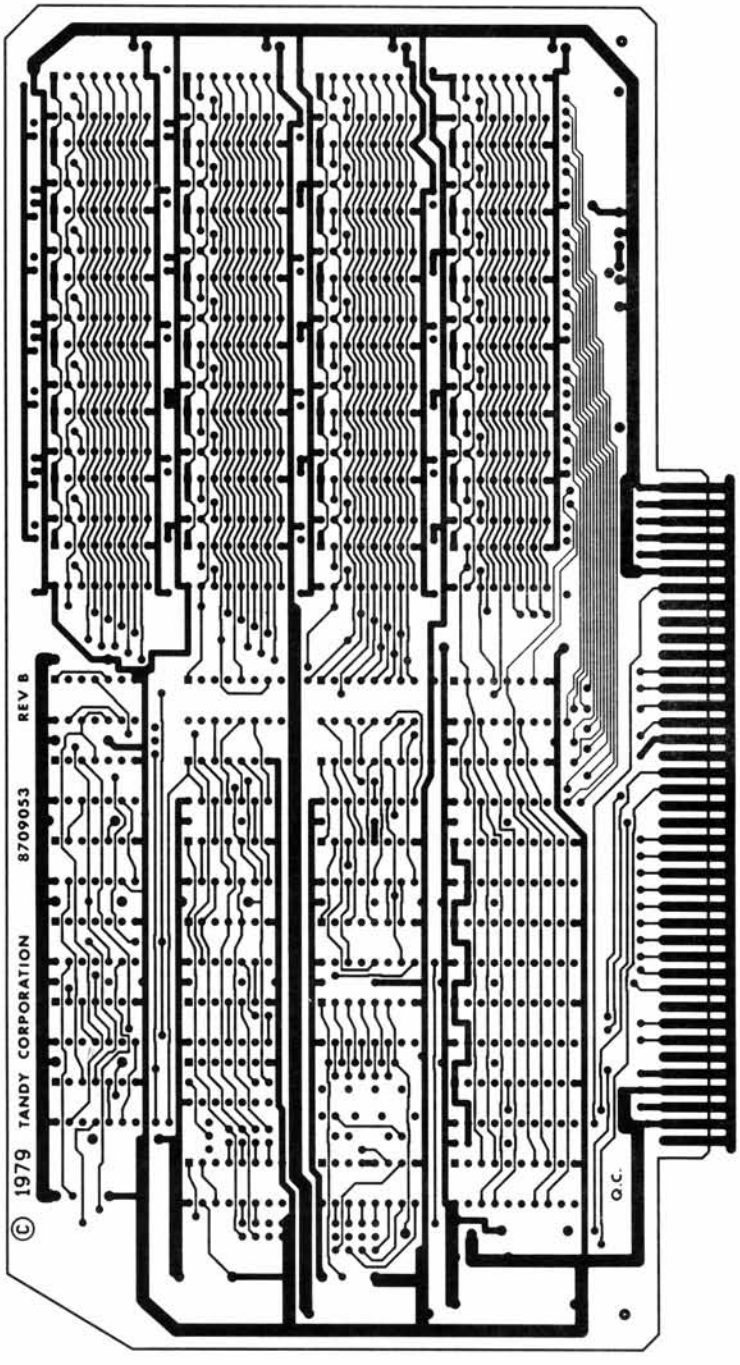




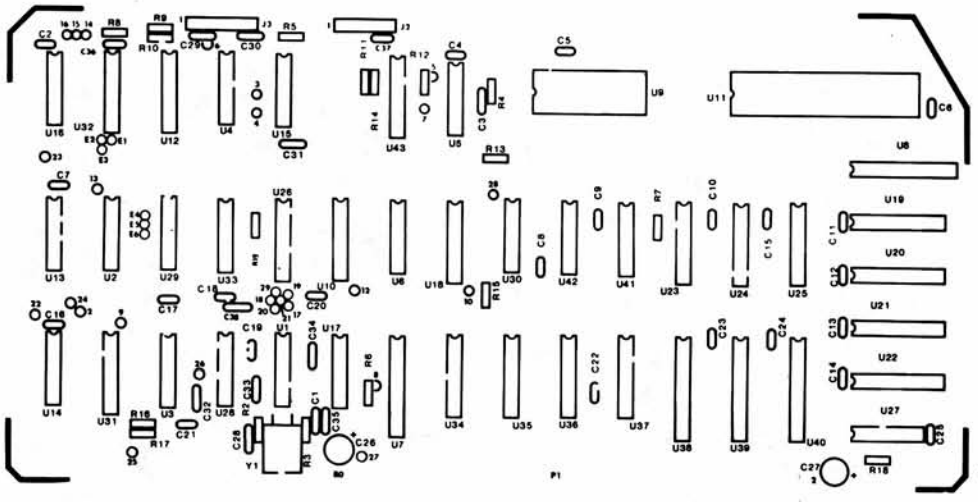
Z8Ø Memory Board



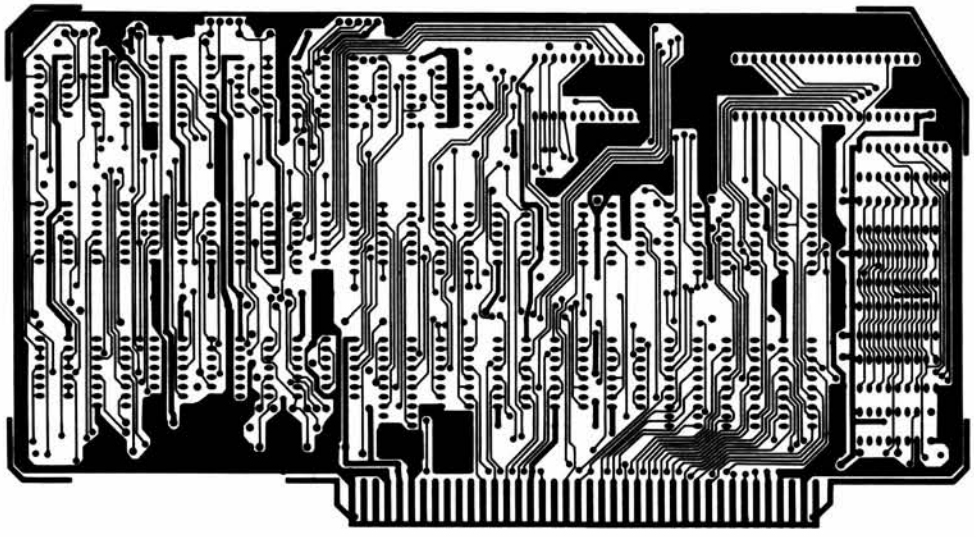



© 1979 TANDY CORPORATION 8709053 REV B
Q.C.

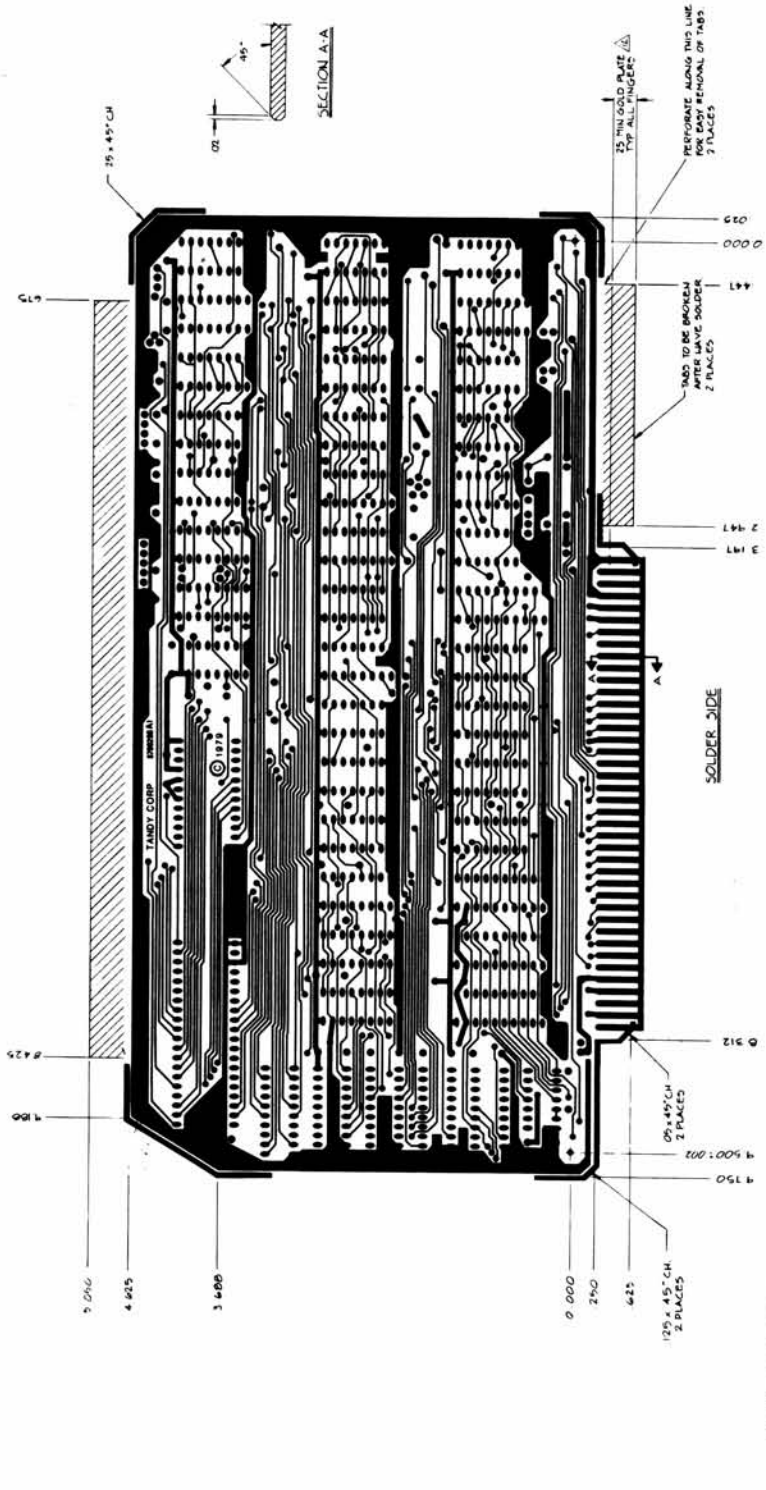
Video Board



SILKSCREEN



COMPONENT SIDE


SECTION A-A
SOLDER SIDE
TANDY CORP
© 1979
.25 MIN GOLD PLATE TYP ALL FINGERS
PERFORATE ALONG THIS LINE FOR EASY REMOVAL OF TABS 2 PLACES
TABS TO BE BROKEN AFTER WAVE SOLDER 2 PLACES
.05 x 45°CH 2 PLACES
.125 x 45°CH 2 PLACES
UNLESS NOTED OTHERWISE:
1. TOOLING HOLES TO BE DRILLED WITH CIRCUIT HOLES
2. HOLE LOCATIONS ON TRUE POSITION .0010
3. ALL HOLE DIA TOLERANCE .003
4. ALL HOLES PLATED THRU WITH .001 THK MIN COPPER
FRONT TO BACK REGISTRATION .002
FINISH SHALL BE 63/37 SOLDER .0005 TO .001 THK
SILKSCREEN TO BE WHITE. PRINT ON COMPONENT SIDE.
SOLDER MASK BOTH SIDES, REGISTRATION .005"
MAT'L SHALL BE NEMA GRADE FR-4
.06 COPPER .002 THK
FINISHED BOARD SHALL MEET UL 94V-0 FLAMMABILITY RATING, TO BE MARKED WITH UL CODE NUMBER
USES SAME DIE AS DRAWING #1000149
PLATE CONTACT FINGERS .000075 GOLD OVER .00020 NICKEL

5/ Parts Lists

Ref. Number	Description	Part Number
	16-Bit CPU Board Subassembly	8898ØØØ
	PC Board CPU (Rev PP3)	87Ø9235
U7	Socket, 2Ø-Pin DIP	85Ø9ØØ9
U11	Socket, 28-Pin DIP	85Ø9ØØ7
U12	Socket, 2Ø-Pin DIP	85Ø9ØØ9
U14	Socket, 2Ø-Pin DIP	85Ø9ØØ9
U15	Socket, 2Ø-Pin DIP	85Ø9ØØ9
U16	Socket, 2Ø-Pin DIP	85Ø9ØØ9
U18	Socket, 2Ø-Pin DIP	85Ø9ØØ9
U22	Socket, 64-Pin	85Ø9Ø14
U33	Socket, 2Ø-Pin DIP	85Ø9ØØ9
U34	Socket, 2Ø-Pin DIP	85Ø9ØØ9
U44	Socket, 2Ø-Pin DIP	85Ø9ØØ9
U49	Socket, 2Ø-Pin DIP	85Ø9ØØ9
U57	Socket, 2Ø-Pin DIP	85Ø9ØØ9
U6Ø	Socket, 2Ø-Pin DIP	85Ø9ØØ9
J1	Header, Dual 25-POS. PCB MT.	8519117
J2	Header, Dual 17-POS. PCB MT.	851912Ø

Capacitors

C1	Ø.1UF 5ØV Mono Axial	8374Ø4
C2	Ø.1UF 5ØV Mono Axial	8374Ø4
C3	Ø.1UF 5ØV Mono Axial	8374Ø4
C4	Ø.1UF 5ØV Mono Axial	8374Ø4
C5	Ø.1UF 5ØV Mono Axial	8374Ø4
C6	Ø.1UF 5ØV Mono Axial	8374Ø4
C7	Ø.1UF 5ØV Mono Axial	8374Ø4
C8	Ø.1UF 5ØV Mono Axial	8374Ø4
C9	Ø.1UF 5ØV Mono Axial	8374Ø4

Ref. Number	Description	Part Number
C1Ø	Ø.1UF 5ØV Mono Axial	8374ØØ4
C11	Ø.1UF 5ØV Mono Axial	8374ØØ4
C12	Ø.1UF 5ØV Mono Axial	8374ØØ4
C13	Ø.1UF 5ØV Mono Axial	8374ØØ4
C14	Ø.1UF 5ØV Mono Axial	8374ØØ4
C15	Ø.1UF 5ØV Mono Axial	8374ØØ4
C16	Ø.1UF 5ØV Mono Axial	8374ØØ4
C17	Ø.1UF 5ØV Mono Axial	8374ØØ4
C18	Ø.ØØ1UF Ceramic 1Ø% Z5P	83Ø21Ø4
C19	Ø.1UF 5ØV Mono Axial	8374ØØ4
C2Ø	Ø.1UF 5ØV Mono Axial	8374ØØ4
C21	Ø.1UF 5ØV Mono Axial	8374ØØ4
C22	Ø.1UF 5ØV Mono Axial	8374ØØ4
C23	Ø.1UF 5ØV Mono Axial	8374ØØ4
C24	Ø.1UF 5ØV Mono Axial	8374ØØ4
C25	Ø.1UF 5ØV Mono Axial	8374ØØ4
C26	27PF 5ØV C.Disk NPO 5%	83ØØ273
C27	1ØØUF 16V Electr. Radial	8327ØØ1
C28	1ØØUF 16V Electr. Radial	8327ØØ1
C29	1ØØUF 16V Electr. Radial	8327ØØ1
C3Ø	1ØØUF 16V Electr. Radial	8327ØØ1
C31	1ØØUF 16V Electr. Radial	8327ØØ1

Resistors

R1	4.7K Ohm 1/4 Watt 5%	827Ø247
R2	2.2K Ohm 1/4 Watt 5%	82Ø7222
R3	4.7K Ohm 1/4 Watt 5%	827Ø247
R4	2.2K Ohm 1/4 Watt 5%	82Ø7222
R5	2.2K Ohm 1/4 Watt 5%	82Ø7222
R6	4.7K Ohm 1/4 Watt 5%	827Ø247
R7	22ØK Ohm 1/4 Watt 5%	82Ø7422
R8	56Ø Ohm 1/4 Watt 5%	87Ø7156
R9	3Ø.1K Ohm 1/4 Watt 1%	82ØØ33Ø
R1Ø	56Ø Ohm 1/4 Watt 5%	87Ø7156
R11	56Ø Ohm 1/4 Watt 5%	87Ø7156
R12	56Ø Ohm 1/4 Watt 5%	87Ø7156
R13	27K Ohm 1/4 Watt 5%	82Ø7327
R14	27K Ohm 1/4 Watt 5%	82Ø7327
R15	27Ø Ohm 1/4 Watt 5%	82Ø7127
R16	51Ø Ohm 1/4 Watt 5%	82Ø7151
R17	56Ø Ohm 1/4 Watt 5%	87Ø7156
R18	4.7K Ohm 1/4 Watt 5%	827Ø247
R19	1ØK Ohm 1/4 Watt 5%	82Ø731Ø

Ref. Number	Description	Part Number
R2Ø	4.7K Ohm 1/4 Watt 5%	827Ø247
R21	22Ø Ohm 1/4 Watt 5%	82Ø7122
RP1	PAK 22Ø-33Ø Ohm SIP	829ØØ2Ø
RP2	PAK 22Ø-33Ø Ohm SIP	829ØØ2Ø
RP3	PAK 22Ø-33Ø Ohm SIP	829ØØ2Ø
RP4	PAK 22Ø Ohm SIP	829Ø122
RP5	PAK 22Ø-33Ø Ohm SIP	829ØØ2Ø
RP6	PAK 22Ø-33Ø Ohm SIP	829ØØ2Ø
RP7	PAK 4.7K Ohm SIP	8294247
RP8	PAK 4.7K Ohm SIP	8294247
RP9	PAK 4.7K Ohm SIP	8294247
RP1Ø	PAK 4.7K Ohm SIP	8293247
RP11	PAK 4.7K Ohm SIP	8294247
C32	1ØØUF 16V Electr. Radial	83271Ø1
C33	68PF 5ØV C.Disk	83ØØ683
C34	68PF 5ØV C.Disk	83ØØ683
C35	68PF 5ØV C.Disk	83ØØ683
C36	1ØØUF 16V Electr. Radial	83271Ø1
C37	1ØØUF 16V Electr. Radial	83271Ø1
C38	1ØØUF 16V Electr. Radial	83271Ø1
C39	1ØØUF 16V Electr. Radial	83271Ø1
C4Ø	1ØØUF 16V Electr. Radial	83271Ø1
C41	68PF 5ØV C.Disk	83ØØ683
C42	1ØØUF 16V Electr. Radial	83271Ø1
C43	1ØØUF 16V Electr. Radial	83271Ø1
C44	1ØØUF 16V Electr. Radial	83271Ø1
C45	1ØØUF 16V Electr. Radial	83271Ø1
C46	1ØØUF 16V Electr. Radial	83271Ø1
C47	1ØØUF 16V Electr. Radial	83271Ø1
C48	1ØØUF 16V Electr. Radial	83271Ø1
C49	22PF 5ØV C.Disk	83ØØ224
C5Ø	Ø.1UF 5ØV Mono Axial	8374Ø4
C51	1ØØUF 16V Electr. Radial	83271Ø1
C52	1ØØUF 16V Electr. Radial	83271Ø1
C53	Ø.1UF 5ØV Mono Axial	8374Ø4
Q1	Transistor 2N29Ø7 PNP	81ØØ9Ø7
Y1	Crystal 24.Ø MHz Quartz .Ø1% HC-18	84Ø9Ø23

Ref. Number	Description	Part Number
Integrated Circuits		
U1	74LSØ8 Quad 2-IN AND 14-Pin	9ØØØØØ8
U2	74LS32 Quad 2-IN OR 14-Pin	9Ø2ØØ32
U3	74SØØ Quad 2-IN NAND 14-Pin	9Ø1ØØØØ
U4	74LS11 Triple 3-IN AND 14-Pin	9Ø2ØØ11
U5	74SØ4 Hex Inverter 14-Pin	9Ø1ØØØ4
U6	74S138 Decoder MUX 16-Pin	9Ø1Ø138
U7	MCM3482B 8-BIT Latch Non-Inv. 2Ø-Pin	8Ø51482
U8	74LS245 Octal Tranceiver 2Ø-Pin	9Ø2Ø245
U9	74LS245 Octal Tranceiver 2Ø-Pin	9Ø2Ø245
U1Ø	74LS374 Octal FLIP-FLOP 2Ø-Pin	9Ø1Ø374
U11	9519A Interrupt Controller AMD 28-Pin	8Ø4Ø519
U12	HAL16R6 Custom Array MMI 2Ø-Pin	8Ø4Ø166
U13	74S138 Decoder MUX 16-Pin	9Ø1Ø138
U14	83Ø3B 8-Bit Transceiver Inv. 2Ø-Pin	8Ø6Ø3Ø3
U15	83Ø3B 8-Bit Transceiver Inv. 2Ø-Pin	8Ø6Ø3Ø3
U16	83Ø3B 8-Bit Transceiver Inv. 2Ø-Pin	8Ø6Ø3Ø3
U17	74LS374 Octal FLIP-FLOP 2Ø-Pin	9Ø1Ø374
U18	83Ø4B 8-Bit Transceiver Non-Inv.	8Ø6Ø3Ø4
U19	74LS51 AND-OR-Inverter 14-Pin	9Ø2ØØ51
U2Ø	74S64 AND-OR-Inverter 14-Pin	9Ø1ØØ64
U21	74LS148 Encoder 16-Pin	9Ø2Ø148
U22	MCM68ØØØ 64-PIN	8Ø4ØØØØ
U23	74LS283 Binary Full Adder 16-Pin	9Ø2Ø283
U24	74LS283 Binary Full Adder 16-Pin	9Ø2Ø283
U25	74S64 AND-OR-Inverter 14-Pin	9Ø1ØØ64
U26	74S64 AND-OR-Inverter 14-Pin	9Ø1ØØ64
U27	74LS11 Triple 3-IN AND 14-Pin	9Ø2ØØ11
U28	74S157 Quad Select MUX 16-Pin	9Ø1Ø157
U29	74S157 Quad Select MUX 16-Pin	9Ø1Ø157
U3Ø	74SØØ Quad 2-IN NAND 14-Pin	9Ø1ØØØØ
U31	74S32 Quad 2-IN OR 14-Pin	9Ø1ØØ32
U32	74LS138 Decoder MUX 16-Pin	9Ø2Ø138
U33	83Ø4B 8-Bit Transceiver Non-Inv.	8Ø6Ø3Ø4
U34	HAL16R6 Custom Array MMI 2Ø-Pin	8Ø4Ø166
U35	74LS374 Octal FLIP-FLOP 2Ø-Pin	9Ø1Ø374
U36	74LS682 8-Bit Comparitor 2Ø-Pin	9Ø2Ø682
U37	74SØ4 Hex Inverter 14-Pin	9Ø1ØØØ4
U38	74LS32 Quad 2-IN OR 14-Pin	9Ø2ØØ32
U39	74LS123 Dual MUX 16-Pin	9Ø2Ø123
U4Ø	74LSØ2 Hex Inverter 14-Pin	9Ø2ØØØ2
U41	74LSØ4 Hex Inverter 14-Pin	9Ø2ØØØ4
U42	74LS125 Tri-State Buffer 14-Pin	9Ø2Ø125
U43	74LS374 Octal FLIP-FLOP 2Ø-Pin	9Ø1Ø374

Ref. Number	Description	Part Number
U44	83Ø4B 8-Bit Transceiver Non-Inv.	8Ø6Ø3Ø4
U45	74LS393 Dual 4-Bit Binary Counter	9Ø2Ø393
U46	74SØ4 Hex Inverter 14-Pin	9Ø1ØØØ4
U47	74S74 Dual FLIP-FLOP 14-Pin	9Ø1ØØ74
U48	74LS74 Dual JK FLIP-FLOP 14-Pin	9Ø2ØØ47
U49	HAL16R8 Custom Array MMI 2Ø-Pin	8Ø4Ø166
U5Ø	7416 Hex Inverter Buffer Driver	9ØØØØ16
U51	74LSØ4 Hex Inverter 14-Pin	9Ø2ØØØ4
U52	74LS244 Octal Buffer 2Ø-Pin	9Ø2Ø244
U53	74LS3Ø 8-IN NAND 14-Pin	9Ø2ØØ3Ø
U54	74S74 Dual FLIP-FLOP 14-Pin	9Ø1ØØ74
U55	74S112 JK NEG. EDGE FLIP-FLOP 16-Pin	9Ø1Ø112
U56	74LS164 Register 14-Pin	9Ø2Ø164
U57	HAL12L6 Custom Array MMI 2Ø-Pin	8Ø4Ø126
U58	74LS32 Quad 2-IN OR 14-Pin	9Ø2ØØ32
U59	74LS3Ø 8-IN NAND 14-Pin	9Ø2ØØ3Ø
U6Ø	MCM3482A 8-Bit Latch Inv. 2Ø-Pin	8Ø5Ø482
U61	74LS244 Octal Buffer 2Ø-Pin	9Ø2Ø244
U62	74LS74 Dual JK FLIP-FLOP 14-Pin	9Ø2ØØ47
U63	74S86 Exclusive-OR 14-PIN	9Ø1ØØ86
U64	74LS174 Hex D-Type FLIP-FLOP 16-Pin	9Ø2Ø174
	16-Bit CPU Board Main Assembly	8898ØØ3
	16-Bit CPU Board Subassembly	8898ØØØ
E2	Jumper Plugs	8519Ø21
E3	Jumper Plugs	8519Ø21
E13	Jumper Plugs	8519Ø21
E14	Jumper Plugs	8519Ø21
16-17, 18-23		
	16-Bit, 128K Memory Board Subassembly	8898ØØ1
	PC Board, Memory 128/256K Rev "PP2"	87Ø9236
U5	Socket, 2Ø-Pin	85Ø9ØØ9
U6	Socket, 2Ø-Pin	85Ø9ØØ9
U7	Socket, 2Ø-Pin	85Ø9ØØ9
U8	Socket, 2Ø-Pin	85Ø9ØØ9
U19	Socket, 14-Pin	85Ø9ØØ8
U2Ø	Socket, 14-Pin	85Ø9ØØ8
U21	Socket, 14-Pin	85Ø9ØØ8
U22	Socket, 14-Pin	85Ø9ØØ8

Ref. Number	Description	Part Number
U3Ø	Socket, 16-Pin	85Ø9ØØ3
U31	Socket, 16-Pin	85Ø9ØØ3
U32	Socket, 16-Pin	85Ø9ØØ3
U33	Socket, 16-Pin	85Ø9ØØ3
U34	Socket, 16-Pin	85Ø9ØØ3
U35	Socket, 16-Pin	85Ø9ØØ3
U36	Socket, 16-Pin	85Ø9ØØ3
U37	Socket, 16-Pin	85Ø9ØØ3
U38	Socket, 16-Pin	85Ø9ØØ3
U39	Socket, 16-Pin	85Ø9ØØ3
U4Ø	Socket, 16-Pin	85Ø9ØØ3
U41	Socket, 16-Pin	85Ø9ØØ3
U42	Socket, 16-Pin	85Ø9ØØ3
U43	Socket, 16-Pin	85Ø9ØØ3
U44	Socket, 16-Pin	85Ø9ØØ3
U45	Socket, 16-Pin	85Ø9ØØ3
U46	Socket, 16-Pin	85Ø9ØØ3
U47	Socket, 16-Pin	85Ø9ØØ3
U5Ø	Socket, 16-Pin	85Ø9ØØ3
U51	Socket, 16-Pin	85Ø9ØØ3
U52	Socket, 16-Pin	85Ø9ØØ3
U53	Socket, 16-Pin	85Ø9ØØ3
U54	Socket, 16-Pin	85Ø9ØØ3
U55	Socket, 16-Pin	85Ø9ØØ3
U56	Socket, 16-Pin	85Ø9ØØ3
U57	Socket, 16-Pin	85Ø9ØØ3
U58	Socket, 16-Pin	85Ø9ØØ3
U59	Socket, 16-Pin	85Ø9ØØ3
U6Ø	Socket, 16-Pin	85Ø9ØØ3
U61	Socket, 16-Pin	85Ø9ØØ3
U62	Socket, 16-Pin	85Ø9ØØ3
U63	Socket, 16-Pin	85Ø9ØØ3
U64	Socket, 16-Pin	85Ø9ØØ3
U65	Socket, 16-Pin	85Ø9ØØ3
U66	Socket, 16-Pin	85Ø9ØØ3
U67	Socket, 16-Pin	85Ø9ØØ3

Resistors

R1	1K Ohm 1/4 Watt 5%	82Ø721Ø
R2	1K Ohm 1/4 Watt 5%	82Ø721Ø
R3	1K Ohm 1/4 Watt 5%	82Ø721Ø
R6	1K Ohm 1/4 Watt 5%	82Ø721Ø
R7	1K Ohm 1/4 Watt 5%	82Ø721Ø
R8	1K Ohm 1/4 Watt 5%	82Ø721Ø

Ref. Number	Description	Part Number
RP1	Network 4.7K Common SIP	8292246
RP2	Network SIP 33 Ohm Series	8295Ø33
RP3	Network SIP 33 Ohm Series	8295Ø33
RP4	Network SIP 33 Ohm Series	8295Ø33
RP5	Network SIP 33 Ohm Series	8295Ø33

Capacitors

C1	Ø.1uF 5ØV Mono Axial	8374Ø4
C2	Ø.1uF 5ØV Mono Axial	8374Ø4
C3	Ø.1uF 5ØV Mono Axial	8374Ø4
C4	Ø.1uF 5ØV Mono Axial	8374Ø4
C5	Ø.1uF 5ØV Mono Axial	8374Ø4
C6	Ø.1uF 5ØV Mono Axial	8374Ø4
C7	Ø.1uF 5ØV Mono Axial	8374Ø4
C8	Ø.1uF 5ØV Mono Axial	8374Ø4
C9	Ø.1uF 5ØV Mono Axial	8374Ø4
C1Ø	Ø.1uF 5ØV Mono Axial	8374Ø4
C11	Ø.1uF 5ØV Mono Axial	8374Ø4
C12	Ø.1uF 5ØV Mono Axial	8374Ø4
C13	Ø.1uF 5ØV Mono Axial	8374Ø4
C14	Ø.1uF 5ØV Mono Axial	8374Ø4
C15	Ø.1uF 5ØV Mono Axial	8374Ø4
C16	Ø.1uF 5ØV Mono Axial	8374Ø4
C17	Ø.1uF 5ØV Mono Axial	8374Ø4
C18	Ø.1uF 5ØV Mono Axial	8374Ø4
C19	Ø.1uF 5ØV Mono Axial	8374Ø4
C2Ø	Ø.1uF 5ØV Mono Axial	8374Ø4
C21	Ø.1uF 5ØV Mono Axial	8374Ø4
C22	Ø.1uF 5ØV Mono Axial	8374Ø4
C23	Ø.1uF 5ØV Mono Axial	8374Ø4
C24	Ø.1uF 5ØV Mono Axial	8374Ø4
C25	Ø.1uF 5ØV Mono Axial	8374Ø4
C26	Ø.1uF 5ØV Mono Axial	8374Ø4
C27	Ø.1uF 5ØV Mono Axial	8374Ø4
C28	Ø.1uF 5ØV Mono Axial	8374Ø4
C29	Ø.1uF 5ØV Mono Axial	8374Ø4
C3Ø	Ø.1uF 5ØV Mono Axial	8374Ø4
C31	Ø.1uF 5ØV Mono Axial	8374Ø4
C32	Ø.1uF 5ØV Mono Axial	8374Ø4
C33	Ø.1uF 5ØV Mono Axial	8374Ø4
C34	Ø.1uF 5ØV Mono Axial	8374Ø4
C35	Ø.1uF 5ØV Mono Axial	8374Ø4
C36	Ø.1uF 5ØV Mono Axial	8374Ø4
C37	Ø.1uF 5ØV Mono Axial	8374Ø4

Ref. Number	Description	Part Number
C38	Ø.luF 5ØV Mono Axial	8374lØ4
C39	Ø.luF 5ØV Mono Axial	8374lØ4
C4Ø	Ø.luF 5ØV Mono Axial	8374lØ4
C41	Ø.luF 5ØV Mono Axial	8374lØ4
C42	Ø.luF 5ØV Mono Axial	8374lØ4

Integrated Circuits

Ul	7438 Quad 2-IN NAND Oprn-C 14-Pin	9ØØØØ38
U2	74LS688 8-Bit Comparator 2Ø-Pin	9Ø2Ø688
U3	74S24Ø Octal Bus Line Driver 2Ø-Pin	9Ø1Ø24Ø
U4	74S24Ø Octal Bus Line Driver 2Ø-Pin	9Ø1Ø24Ø
U5	MCM3482A 8-Bit Latch 2Ø-Pin	8Ø5Ø482
U6	MCM3482A 8-Bit Latch 2Ø-Pin	8Ø5Ø482
U7	MCM3482A 8-Bit Latch 2Ø-Pin	8Ø5Ø482
U8	MCM3482A 8-Bit Latch 2Ø-Pin	8Ø5Ø482
U9	74S24l Octal Bus Line Driver 2Ø-Pin	9Ø1Ø241
U1Ø	7525 Dual 4-IN NOR 14-Pin	9ØØØØ25
U11	74LS32 Quad 2-IN OR 14-Pin	9Ø2ØØ32
U12	74S74 Dual JK FLIP-FLOP 14-Pin	9Ø1ØØ74
U13	DDU4-52ØØ Delay Line (2ØØns) 14-Pin	8429Ø1Ø
U14	74LS393 Dual 4-Bit Binary Counter	9Ø2Ø393
U16	74SØ4 Hex Inverter 14-Pin	9Ø1ØØØ4
U17	74SØØ Quad 2-IN NAND 14-Pin	9Ø1ØØØØ
U18	74SØØ Quad 2-IN NAND 14-Pin	9Ø1ØØØØ
U23	74SØ8 Quad 2-IN AND 14-Pin	9Ø1ØØØ8
U24	74S1Ø Triple 3-IN NAND 14-Pin	9Ø1ØØ1Ø
U25	74S1Ø Triple 3-IN NAND 14-Pin	9Ø1ØØ1Ø
U26	74SØ4 Hex Inverter 14-Pin	9Ø1ØØØ4
U15	74S37 Quad 2-IN NAND Buffer 14-Pin	9Ø1ØØ37
U27	74S74 Dual JK FLIP-FLOP 14-Pin	9Ø1ØØ74
U28	74S157 Quad 2-IN MUX 16-Pin	9Ø1Ø157
U29	74S157 Quad 2-IN MUX 16-Pin	9Ø1Ø157
U48	74S157 Quad 2-IN MUX 16-Pin	9Ø1Ø157
U49	74S157 Quad 2-IN MUX 16-Pin	9Ø1Ø157
U5Ø	MCM6665 Dynamic RAM (2ØØns) 16-Pin	8Ø4Ø665
U51	MCM6665 Dynamic RAM (2ØØns) 16-Pin	8Ø4Ø665
U52	MCM6665 Dynamic RAM (2ØØns) 16-Pin	8Ø4Ø665
U53	MCM6665 Dynamic RAM (2ØØns) 16-Pin	8Ø4Ø665
U54	MCM6665 Dynamic RAM (2ØØns) 16-Pin	8Ø4Ø665
U55	MCM6665 Dynamic RAM (2ØØns) 16-Pin	8Ø4Ø665
U56	MCM6665 Dynamic RAM (2ØØns) 16-Pin	8Ø4Ø665
U57	MCM6665 Dynamic RAM (2ØØns) 16-Pin	8Ø4Ø665
U6Ø	MCM6665 Dynamic RAM (2ØØns) 16-Pin	8Ø4Ø665
U61	MCM6665 Dynamic RAM (2ØØns) 16-Pin	8Ø4Ø665

Ref. Number	Description	Part Number
U62	MCM6665 Dynamic RAM (200ns) 16-Pin	8040665
U63	MCM6665 Dynamic RAM (200ns) 16-Pin	8040665
S1	SWitch, DIP 8-Pos 16-Pin	8489004
	16-Bit, 128K Memory Board Main Assembly	8898002
	Model 16 Memory Board Subassembly	8898001
U64	MCM6665 Dynamic RAM (200ns) 16-Pin	8040665
U65	MCM6665 Dynamic RAM (200ns) 16-Pin	8040665
U66	MCM6665 Dynamic RAM (200ns) 16-Pin	8040665
U67	MCM6665 Dynamic RAM (200ns) 16-Pin	8040665
E1	Jumper Plug	8519021
E2	Jumper Plug	8519021
E13	Jumper Plug	8519021
E14	Jumper Plug	8519021
E16	Jumper Plug	8519021
E17	Jumper Plug	8519021
E18	Jumper Plug	8519021
E19	Jumper Plug	8519021
E20	Jumper Plug	8519021
E21	Jumper Plug	8519021
E22	Jumper Plug	8519021
E23	Jumper Plug	8519021
	Cable, 34 Pos. Int. Bus. Ext. II	8709278
	Cable, 50 Pos. Int. Bus. Ext. II	8709279

Mechanical Parts List

Description	Part Number
Keyboard	879Ø516
Case, KB Upper	8719198
Case, KB Lower	8719199
Harness, INT	87Ø9277
Logo, MOD 16 KB	8719183
Screw, #6 X 3/4" PPH T	8569Ø29
Label, KB ID	878964Ø
Label, KB SN	8789634
Foot, Rubber KB	8589ØØ5
Diskette, TRSDOS 2.Øb P/A	8898Ø42
Cord, Power 8'	87Ø9Ø57
Kit, CPU Power Cord	88938ØØ
Base Plate, Chassis	8729133
Fan, 11ØV	879Ø5Ø5
Screw, #632 X 1 13/16	8569Ø73
Nut, Lock #632	8579ØØ4
Washer, #8 Star	8589Ø27
Screw, #832 X 3/4" HEX HD	8569148
Wire, GRD A/C M16	87Ø93Ø3
Wire, GRD CONN BRKT	87Ø93Ø4
Nut, Lock #832	8579Ø28
Wire, Harness AC	87Ø93Ø5
Switch, Power ON/OFF	8489Ø39
Screw, #6 X 1/2" PPH TB ZN	8569Ø39
Tie, 7" Nylon Cable	859ØØ87
Screw, #8 X 3/8"	8569Ø54
Bracket, Bezel Lower	8729189
Bracket, VID MTG	9729Ø1Ø
Bracket, Bezel Upper	8729185
Bracket, Floppy Disk	8729182
Panel, Rear Connector	8729184
Cable, FDC Disk Bus	87Ø9269
Plate Adaptor	9729Ø17
Screw, #6 X 5/16"	856913Ø
Cover, Bottom OPO1Ø	8898Ø34
Plug	8729125
Connector, A/C Power	8519Ø13
Screw, #44Ø X 1/2" PPH BL	8569Ø33
Nut, Lock #44Ø	8579ØØ3
Cable, Serial I/O	87Ø9Ø56

Description	Part Number
Screw, Lock Assy	8569101
Screw, #632 X 1/2" PPH BLK	8569126
Nut, Lock #632	8579004
Cover, Bottom OPO20	8898035
Screw, #440 X 1/2" PPH BL	8569033
Nut, Lock #440	8579003
Cable, Parallel I/O	8709298
Bracket, GRD	8709302
Strap, GRD	8709306
Tab, Faston GRD M16	8529038
Cover, Bottom OPO30	8898036
Case, Bottom MOD 16	8719200
Feet, Rubber	8590072
Screw, #4 X 3/8" Plastite	8569102
Screw, #832 X 1/2" PPH	856905O
Nut, Lock #832	8579028
Tab, Plastic 1" X 1" BL	8719126
Cover, Bottom OPO40 F/A	8898037
Clamp, Chassis	8729128
Screws, #832 X 1/2" PPH ZN	8569078
Nut, #832 X 3/8"	8579028
Kit, 12" CRT Display	8790606
Shield, Wire X 7"	8440001
Tubing, PVC 9/32 D. X 6 1/2	8539023
Tubing, Shrink	8539024
CRT Display (Reworked)	8898021
OPO 30 M16 1DR	8898110
PWR Supply (13 AMP)	8790040
Harness, DC Wiring	8709282
Harness, Video	8709300
Potentiometer, 500K Brightness	8262450
Potentiometer, 500 Ohm Contrast	8261150
Screw, #832 X 3/4" PPH	8569097
Washer, .625OD .203F	8589055
Nut, Lock #832	8579028
Label, UL Warning	8789680
Screw, #440 X 3/4" ZN	8569059
Tab, Faston GRD M16	8529038
Washer, #4 Lock	8589021
Washer, #4 Flat	8589002
Screw, #8 X 3/8" ZN HEX Slot	8569054
OPO40 M16 1DR	8898112
Disk Drive	8790119
Shield, Disk Drive	8729126
Strap, Front Drive	8729100
SCR, #832X1/4 LN 82 DEG FL ZN	8569141
Strap, Rear Drive	8729101

Description	Part Number
Bracket, Tie Down	8729103
Drive Assy, M16 1DR	8898102
CPU PCB, S/A 8-Bit	8898020
Label, CPU S/N	8789084
IC 2716 EPROM	8040716
IC, Z80A CPU	8047880
IC, Z80A DMA	8047883
IC, Z80A CTC	8047882
IC, Z80A SIO	8047884
Plug Jumper	8519021
CPU, 8-Bit Assembly	8898023
CPU, 8-Bit Visual	8898023
CPU, 8-Bit Testing	8898023
CPU, 8-Bit Repair	8898023
CPU PCB, 8-Bit F/A	8898023
CPU PCB, S/A 16-Bit	8898000
Label, CPU S/N	8789632
IC, PAL 12L6 CSM ARY (U57)	8040126
IC, 12L6 CSM ARY (U57) PROGM.	8898014
IC, PAL 16R6 CSM ARY (U12)	8040166
IC, 16R6 CSM ARY (U12) PROGM.	8898013
IC, PAL 16R6 CSM ARY (U34)	8040166
IC, 16R6 CSM ARY (U34) PROGM.	8898012
IC, 16R8 CSM ARY (U49)	8040168
IC, 16R8 CSM ARY (U49) PROGM.	8898015
IC, 9519A Interrupt Controller	8040519
IC, MC68000 MPU (U22)	8040000
Jumper Plugs	8519021
CPU, 16-Bit Assembly	8898003
CPU, 16-Bit Visual	8898003
CPU, 16-Bit Testing	8898003
CPU, 16-Bit Repair	8898003
CPU PCB, 16-Bit F/A	8898003
FDC PCB, Subassy	8898019
Jumper Plugs	8519021
IC, Z80PIO Parallel I/O CONTR	8047881
IC, WD179102 Floppy Formatter	8045791
IC, WD1691 Floppy Formatter	8040691
IC, WD214301 4-Phase Clock	8040143
64K MEM PCB Assy	8893498
Label, MEM S/N	8789086
Plug Jumper	8519021
IC, 200ns 16K RAMs	8040016
128K MEM PCB Assy	8898001
Label, 128K S/N	8789631
IC, MCM6665 Dynamic RAM (200ns)	8040665
Jumper Plugs	8519021

Description	Part Number
PCB, 128K MEM F/A	8898ØØ2
Video PCB Assy	8898Ø18
Label, VID S/N	8789Ø87
Jumper Plug	8519Ø21
IC, 6845 CRT Control	8Ø5Ø845
IC, 2316 ROM	8Ø43316
IC, 2114 Static RAM	8Ø43114
Bracket, PC Left Side	8729115
Bracket, PC Right Side	9729Ø11
Screw, #632 X 3/8" FIL	8569Ø71
Washer, #6 Lock ZN	8589Ø18
Screw, #832 X 3/8"	8569Ø3Ø
Harness, RESET Switch	87Ø93Ø1
Clamp, Cable	8559Ø36
Screw, #6 X 1/4"	8569Ø4Ø
Washer, #8 Flat	8589Ø16
Washer, #8 Nylon Flat	8589Ø22
Nut, #8 HEX	8579Ø13
Card Cage Mech Assy	8898Ø25
Bracket, PC Retain	9729Ø14
Spacer, Plastic	8589Ø14
Rivet, Pop 1/8X	8559ØØ7
Washer, #8 Flat	8589Ø16
Nut, #632 HEX ZN	8579Ø14
Cable, INT Disk	87Ø928Ø
Cable, INT 34 POS BUS	87Ø9278
Cable, INT 5Ø POS BUS	87Ø9279
Card Cage, FA M16 1DR	8898ØØ
Screw, #8 X 3/8" SHT MTL HEX HD	8569Ø54
Label, FCC ID M16 1DR	8789657
Label, S/N CPU M16 1DR	8789637
Label, Part 15 FCC	8789287
Clamp, Cable	8559Ø36
Screw, #832 X 3/8"	8569Ø3Ø
Tie, 5" Nylon	859ØØ95
Screw, #832 X 1/4"	8569Ø36
Screw, #8 X 3/8" ZN	8569Ø54
Washer, #8 Star	8589Ø27
Screw, #832 X 1/4"	8569Ø36
Washer, #8 Star	8589Ø27
Clip Cord, 52" DIA	8559Ø15
Clip Cord, 38" DIA	8559Ø1Ø
Switch, Momentary	8489Ø4Ø
Capacitor, .ØØ47UF, 2Ø% 5ØV	83Ø2473
Switch, RESET F/A	8898Ø5Ø
Clamp, Cable	8559Ø36
OPO5Ø M16 1DR	8898111

Description	Part Number
OPO6Ø M16 1DR Mech Insp.	8898111
OPO7Ø M16 1DR Test	8898111
OPO8Ø M16 1DR Burnin	8898111
Plate Name, MOD 16	8719194
Bezel, Front MOD 16	8719192
Bezel, Overlay	8719188
Clip	8729107
Nut, 3/8"32 Steel	8579023
Knob, CONT 1 BRT	859ØØ7Ø
Cable, KEYBD External	87Ø9299
Screw, #4 X 1/4" Plastite	8569Ø32
Screw, #8 X 1/2" PPH T	8569Ø56
Washer, .625OD X .2Ø3 ID	8589Ø55
Washer, #8 Flat	8589Ø16
Screw, #832 X 3/8"	8569Ø3Ø
Tie, 5" Nylon	859ØØ95
Tab, Plastic 1" X 1"	8719126
Case, Upper MOD 16 C	8719201
Screw, #832 X 1/2" PPH	8569Ø5Ø
Insert, Disk Protector	8779Ø96
CPU, MOD 16 Final Assy	8898114
OPO9Ø M16 1DR Burnin	8898114
OPO1ØØ M16 1DR Test	8898114
OPO11Ø M16 1DR Q.C.	8898114
OPO12Ø M16 1DR Q.A. Test	8898114

6/ Schematics

68ØØØ CPU Board

128K/256K Memory Board

Z8Ø CPU Board

Floppy Disk Board

Z8Ø Memory Board

Video Board

ZONE	LTR	REVISION DESCRIPTION	DATE	APPROVED

UPPER DATA BUFFERING

LS245

TO Z80 BUS

J0-P51 D00 → BD0# J1-P10 → RP6/6
J0-P52 D01# → BD1# J1-P8 → RP5/6
J0-P53 D02# → BD10# J1-P12 → RP6/7
J0-P54 D03# → BD11# J1-P11 → RP5/7
J0-P55 D04# → BD12# J1-P14 → RP6/8
J0-P56 D05# → BD13# J1-P13 → RP5/8
J0-P57 D06# → BD14# J1-P16 → RP6/9
J0-P58 D07# → BD15# J1-P15 → RP5/9

TO 68K BUS

D6 UDEN# → U8
B5 BR/W# → U8

LOWER DATA BUFFERING

LS245

TO Z80 BUS

J0-P51 D00# → BD0# J1-P2 → RP6/2
J0-P52 D01# → BD1# J1-P1 → RP5/2
J0-P53 D02# → BD2# J1-P4 → RP6/3
J0-P54 D03# → BD3# J1-P3 → RP5/3
J0-P55 D04# → BD4# J1-P6 → RP6/4
J0-P56 D05# → BD5# J1-P5 → RP5/4
J0-P57 D06# → BD6# J1-P8 → RP6/5
J0-P58 D07# → BD7# J1-P7 → RP5/5

TO 68K BUS

C6 LDEN# → U5 EN#
B5 BR/W# → U5 DIR

ADDRESS GEN CONT.

Z80 BUS

J0-P30 A7# → BA7# J1-P33
J0-P29 A6# → BA6# J1-P34
J0-P28 A5# → BA5# J1-P31
J0-P27 A4# → BA4# J1-P32
J0-P26 A3# → BA3# J1-P29
J0-P25 A2# → BA2# J1-P30
J0-P24 A1# → BA1# J1-P28
J0-P23 A0# → 9

TO 68K BUS

B5 BUSGQ# → 19 US2 LS244

ADDRESS AND CONTROL GEN.

Z80 BUS

J0-P58 D7# → 3D → 3Q → BA22# J1-P50
J0-P57 D6# → 4D → 4Q → BA21# J1-P47
J0-P56 D5# → 7D → 7Q → BA20# J1-P48
J0-P55 D4# → 8D → 8Q → BA19# J1-P45
J0-P54 D3# → 5D → 5Q → BA18 J1-P46
J0-P53 D2# → 6D → 6Q → BA17# J1-P43
J0-P52 D1# → 7D → 7Q → BA16# J1-P44
J0-P51 D0# → 8D → 8Q → BA15# J1-P41

TO 68K BUS

B5 OUTDF → 11
B5 BUSGQ# → 1 G# U7 MC3662B

J0-P58 D7# → 13 INVERTING → 12 → LA14 C2
J0-P57 D6# → 8 → 9 → CONT6#DI7
J0-P56 D5# → 14 → 15 → CONT5#DI7
J0-P55 D4# → 7 → 6 → CONT4#DI7
J0-P54 D3# → 17 → 16 → RESET C10,C6
J0-P53 D2# → 4 → 5 → HALT D16
J0-P52 NC → 18 → 19 → NC
J0-P51 D0# → 3 → 2 → CONT0 C5

Z80 BUS

B5 OUTDE → 11
1 → EN# U6B AC3482A

68K CONTROL

C5 LA14 → U4C S04 → 9

J0-P36 A13# → 13 → BA13# J1-P39
J0-P35 A12# → 15 → BA12# J1-P40
J0-P34 A11# → 6 → BA11# J1-P37
J0-P33 A10# → 17 → BA10# J1-P38
J0-P32 A9# → 4 → BA9# J1-P35
J0-P31 A8# → 2 → BA8# J1-P36

8 → 12 NC

TO 68K BUS

B5 BUSGQ# → 1 → 19 U61 LS244

J0-P30 A7# → U51 → BA7# J1-P33
J0-P29 A6# → U51 → BA6# J1-P34
J0-P28 A5# → U51 → BA5# J1-P31
B6 HI → U63 S86
J0-P27 A4# → U51 → BA4# J1-P32
J0-P26 A3# → U51 → BA3# J1-P29
J0-P25 A2# → U51 → BA2# J1-P30
J0-P24 A1# → U51 → BA1# J1-P28

Z80 BUS

74LS30 U59

(J0-P22) Z80 IORQ# → U58 32
(J0-P20) Z80 WR# →

(J0-P23) Z-80 AB# → U41 04 → U58 32 → U41 04 → OUTDE C2

U58 32 → U41 04 → OUTDF B2

COMPONENT SIDE

Z(1) J1 Z
J2 J3
34(33)
Z(1) 79(80)
J1
50(49)

4.7K RP10 +5V

WAITREQ HI → 1
Z80BUSAK HI → 2
C4 ADDVAL → 3
Z80 RD# → 4
Z80 WR# → 5
→ 6
C5 BG1# → 7
C9 BDTACK# → 8
MEMSEL# → 9
GND → 10

WAIT# (J0-P40) Z80 C5
BR/W# C5,C1,D1,C13
BUSGQ# B2,D2
BRI#
BAS# C8,D14
BUDS# D5,C13
BLDS# D5,C13
BG1# C4,C5
CONT0 C3

WALIER6 U34 SS006 VCC Q7 Q6 Q5 Q4 Q3 Q2 Q1 I/O E#

U42 125 U42 125 U42 125 U42 125 U42 125 U42 125

C6 CONT1# → 5
B9 MREQ# (J0-P21) Z80 → 4
U58 32 → 6

(J0-P37) A14# Z80 → U1 08 → ADDVAL D4
(J0-P36) A13# Z80 → U41 04

B5 BR/W# → U2 32
C5 BG1# →
C5 BLDS# → U2 32
C5 BUDS# → U2 32

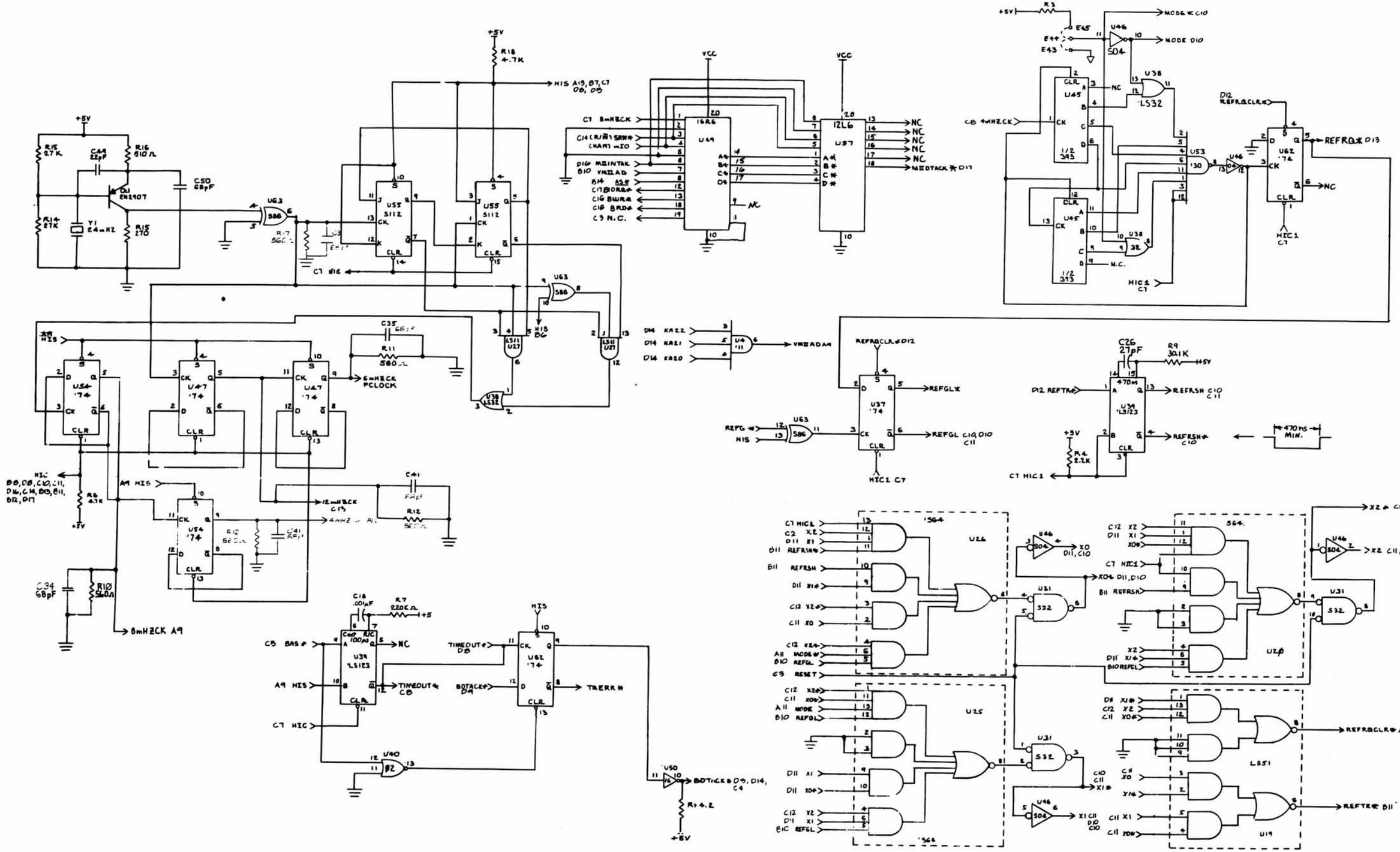
U1 08 → LDEN# D1
U1 08 → UDEN# B1

HI A4,B9,C13,D13

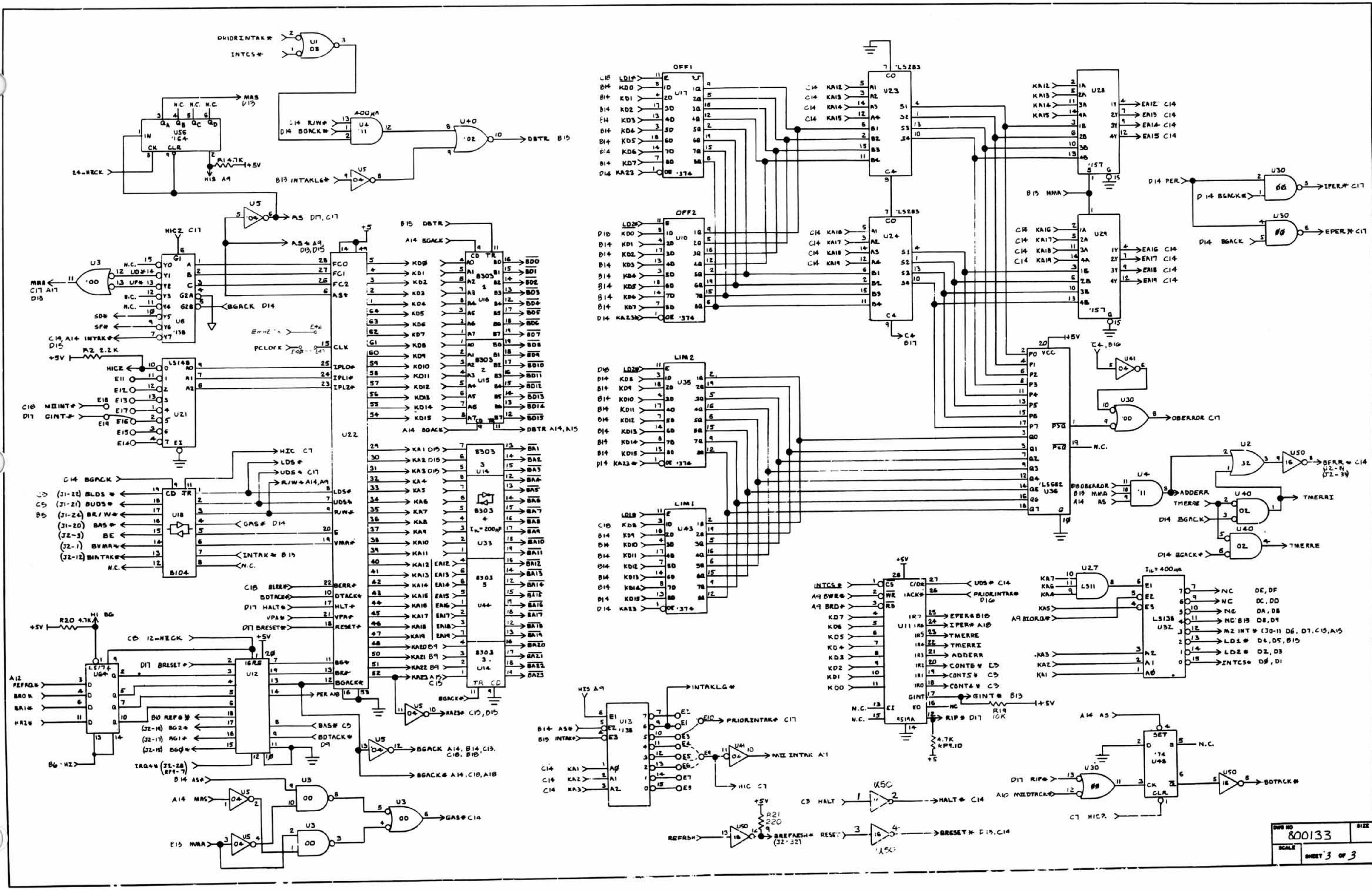
U48 74LS74 D Q CK CLR

(J0-P52) D1# Z80 → 12
OUTDE → 11
10 → NC.
9 → CONT1#C9
13 → RESET# (J0-P47) Z80 C5

MATERIAL	UNLESS OTHERWISE SPECIFIED			DRAFT	DATE	TITLE
	TOLERANCES .XX = ±.010 .XXX = ±.005 ANGLES = ±1° HOLE DIA TOLERANCES .014 - .250 = +.005 -.001 .251 - .750 = +.008 -.001 .751 - UP = +.015 -.001			CHECK	DATE	MODEL 16 CPU
				DESIGN	DATE	
FINISH				APPD	DATE	
				APPD	DATE	LAST UPDATE: 5-18-82
	DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING			tandy		DWG NO 80C033
	DO NOT SCALE THIS DRAWING	NEXT ASSY	USED ON			SCALE SHEET OF 3



DWG NO. 800133	SIZE
SCALE	SHEET 2 OF 3


DWG NO
800133
SIZE
SCALE
SHEET 3 OF 3

ZONE	LTR	REVISION DESCRIPTION	DATE	APPROVED

COMPONENT SIDE

J2 J0 J1

A0 A1 A2 A3 A4 A5 A6 A7

R/W UPPER BYTE

CASU

R/WG

UDSG

LDSG

RAS, U

RAS, L

R/W LOWER BYTE

CASL

AMUX

A3

+5V

R8

U18 S00 S04

U16 348ZA INVERTING

U20 U21 S280

MCM6665

D8 D9 D10 D11 D12 D13 D14 D15 P0 P1

U36 U35 U34 U33 U32 U31 U30 U38

U57 U56 U55 U54 U53 U52 U51 U50 U58

U47 U46 U45 U44 U43 U42 U41 U40 U39

U67 U66 U65 U64 U63 U62 U61 U60 U59

D0 D1 D2 D3 D4 D5 D6 D7 PL

20000-3FFFF

0-1FFFF

U5 U8 U19 U22 348ZA

U17 S00 U26 S04 U27 S74 U1 S38

R1 R7 TP1

HI UL1

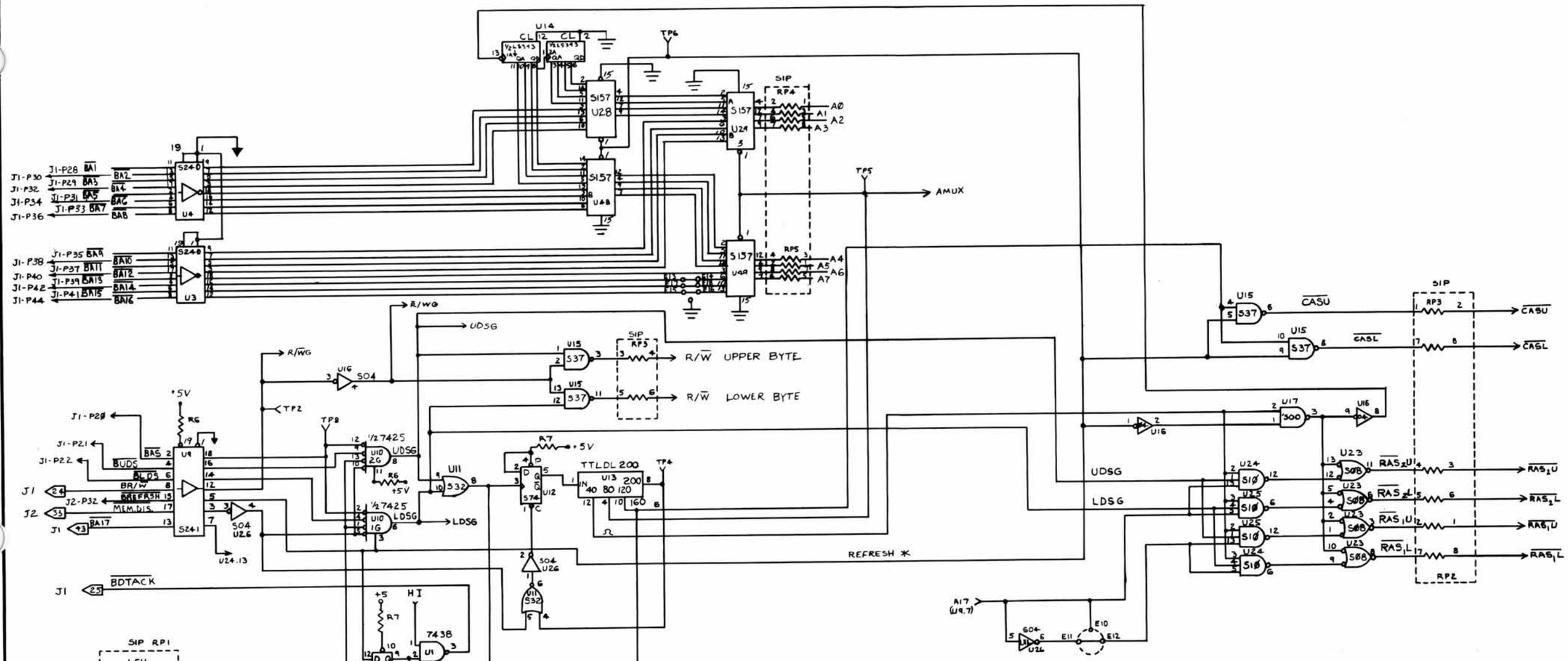
INT

E8 E7 E6 E5 E4 E3 E2 E1

J2 24 25 26 27 28 29 30 31

MATERIAL	UNLESS OTHERWISE SPECIFIED			DRAFT Tom Casteel	DATE 6-10-81	TITLE MODEL 16-BIT MEMORY BRD	
FINISH	TOLERANCES .XX = ±.010 .XXX = ±.005 ANGLES = ±1° HOLE DIA TOLERANCES .014 - .250 = +.005 -.001 .251 - .750 = +.008 -.001 .751 - UP = +.015 -.001			CHECK	DATE		
				DESIGN	DATE		
				APPD	DATE		
				APPD	DATE	REV PP3	
	DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING			tandy	1-5-82	DWG. NO. 8000127	SIZE D
	DO NOT SCALE THIS DRAWING	NEXT ASSY.	USED ON 402			SCALE	SHEET 1 OF 2

ZONE	LTR	REVISION DESCRIPTION	DATE	APPROVED



MATERIAL	UNLESS OTHERWISE SPECIFIED			DRAFT TOM CASTELLON	DATE
	TOLERANCES .XX = ± .010 .XXX = ± .005 ANGLES = ±1° HOLE DIA TOLERANCES .014 - .250 = +.005 -.001 .251 - .750 = +.008 -.001 .751 - UP = +.015 -.001			CHECK	DATE
				DESIGN	DATE
FINISH				APPD Jimmy Johnson	DATE 2/22/82
				APPD	DATE
	DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING				
	DO NOT SCALE THIS DRAWING	NEXT ASSY.	USED ON 402		

TITLE: MODEL 16 - BIT MEMORY BOARD

REV PP3 1-5-82

tandy

DWG NO. 8000127 SIZE D

SCALE SHEET 2 OF 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	V. TERRY 1. MOVED TP6, ADDED PIN NUMBERS 12 AND 13 TO LS04, U29	8-17-79	
A7,8	B	V. TERRY 1 REDESIGN POWER ON AND MANUAL REBET LOGIC	9-21-79	
B2	C	T.C. 1. ADDED U21,32...U15,00...U24 2. ADDED JUMPER PIN NUMBERS.	12-15-81	
B5 6	D	T.C. 1. DELETED CLOCK OPTION. 2. ADDED C48, C47, C46, R31 & R33	12-28-81	

U12 Z80A CPU

U20 Z80A DMA

U11 2716 EPROM

U35 LS240

U34 LS240

U17 LS04

U33 LS244

U21 32

U15 00

U24

U4 LS00

U3 32

U30 LS132

U29 LS04

U1 LS04

U2 LS74

LS125 1139

Y1

Q1 2N3906 PNP

CLOCK LOGIC

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TOLERANCES: FRACTIONAL ± 1/64
ANGLES ± 1°
TWO PLACE DECIMAL ± .010
THREE PLACE DECIMAL ± .005
DO NOT SCALE THIS DRAWING

NEXT ASSEMBLY | USED ON | APPLICATION

MATERIAL

DRAWN Michael Wright DATE
CHECKED DATE
DESIGN ENGINEER SAM SANTYBE DATE
PROJECT ENGINEER DATE
CHIEF ENGINEER DATE
MANUFACTURING DATE
GENERAL MANAGER DATE

tandy SYSTEMS DESIGN
2725 West Seventh Street Fort Worth, Texas 76107

TITLE
CPU MODULE
MODEL II

SIZE D | DRAWING NO. 800005 1 | REV D

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
B,C,B	A	ADDED U4 DESIGNATION -TC	12-28	
C5	B	DELETED JUMPER PINS E13 - E15	12-28	

Z80A CTC U19

Z80A SIO/0 U18

J1

RECEIVED DATA CH.A
RECEIVER CLOCK CH.A
TRANSMIT CLOCK CH.A
DATA SET READY CH.A
CLEAR TO SEND CH.A.
CARRIER DETECT CH.A
XMIT DATA CH.A
REQUEST TO SEND CH.A
DATA TERM. RDY CH.A
RECEIVED DATA CH.B
RECEIVER XMITTER CLK. CH.B
DATA SET READY CH.B
CLEAR TO SEND CH.B
CARRIER DETECT CH.B
TRANSMIT DATA CH.B
REQUEST TO SEND CH.B
DATA TERMINAL READY CH.B

4 TEST POINTS THIS SHEET TP9 → TP12

FROM Z80A CPU

TO CPU RESET PIN 26

INTRQL*, SH.1

Z80 DMA, PIN 38 PAGE 1

Z80 DMA, PIN 36 PAGE 1

EIOUT TO IE IN PIN 19 BUS

KBIRQ J0-P42

TO ½ Φ SHEET 1

CECTC*

CESIO*

XMIT S.E.T.

WAIT* (TO CPU) P24 CPU

WAIT* (FROM BUS) J0, P48

RESET* P26 CPU

ROM*/ RAM, SH.3

SHADOW*

ROM/RAM*

MINAIT*

OBWAIT*

M1* SH.1

Φ SH.1

MREQ* SH.1

POWER ON AND MANUAL RESET LOGIC

RESET* (TO CPU AND BUS, PG 1)

DPDT MOM. CONT SWITCH

4 POSITION HEADER

NEXT ASSEMBLY	USED ON	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: FRACTIONAL ± 1/64 ANGLES ± 1° TWO PLACE DECIMAL ± .010 THREE PLACE DECIMAL ± .005 DO NOT SCALE THIS DRAWING	DRAWN Michael Wigal	DATE 1-2-79	tandy SYSTEMS DESIGN 2725 West Seventh Street Fort Worth, Texas 76107
APPLICATION		MATERIAL	CHECKED	DATE	TITLE CPU MODULE MODEL II
			DESIGN ENGINEER SAM SANYER	DATE	SIZE D DRAWING NO. 8000051 REV D
			PROJECT ENGINEER	DATE	SCALE SHEET 2 OF 2
			CHIEF ENGINEER	DATE	
			MANUFACTURING	DATE	
			GENERAL MANAGER	DATE	

BUSSED DATA LINES FROM Z80A CPU

A7 A6 A5 A4 A3 A2 A1 A0

U37 LS20 · U38 LS32 · U38 LS32 · 74LS145 U36

+5V

2.2 R26 · 2.2 R29 · 2.2 R27 · 2.2 R28

F9* · F8* · F4→F7* · F0→F3*

CEDMA* S1 · CECTC* S2 · CESIO* S2

U37 LS20 · U17 I/O ADD* · U16 LS32 · U14 LS08 · TP15 · SELECT* SH.1

R31 1.2K · C47 220pF

RD* · IORQ* · WR*

U5 LS32 · U5 LS32 · U14 LS08 → IN*, LS10 · IN*+OUT*

U3 LS32 → OUT F9* SHADON*

ROM*/RAM SH2.

A15* · A14* · A13* · A12* · A11*

U38 LS32 · U5 LS32 · U38 LS32 · U5 LS32 · TP18 · LOW 4K* · U17 · U16 LS32 · U16 LS32 · U16 LS32

ROMBCE*, SH.1 · ROMICE*, N.C · RDROM*

RD* · MREQ* · U3 LS32 · READ* · TP4 · TO ROM OE

DMA EXT* SH.1

BUSRQ*(BUS) · BAO(DMA CHIP), S1. · U3 LS32

U14 LS08 · TP17 · TP16

IEO · U21 LS32 · LOCAL INT. PENDING · U22 LS10

M1* · IORQ* · U21 LS32 · INTAK* · TP13

READ* · INTAK* · IN* · SELECT* · U22 LS10

FROM Z80A CPU BUSSED LINES

+12V · -12V

U32 BT26A

D0 D1 D2 D3 D4 D5 D6 D7

DE · RE* · U31 BT26A

DAT0* 51 · N.C. USER0 1 · N.C. USER1 2 · DAT1* 52 · IE OUT,SH2 14 · DAT2* 53 · EIIN 13 · BAKIN* 15 · DAT3* 54 · BUSRQ* 17 · DAT8* 59 · DAT9* 60 · DAT10* 61 · DAT11* 62 · DAT12* 63 · DAT13* 64 · DAT14* 65 · DAT15* 66 · DAT4* 55 · +5V 72 · +5V 71 · DAT5* 56 · +5V 10 · +5V 9 · DAT6* 57 · N.C. RES. 39 · DISRO* 40 · KBIRQ* 42 · DAT7* 58 · WAIT*(BUS) 48 · RTC,SH.2 67

3 4 7 8 49 50 69 70 73 74 79 80

J0

6 TEST POINTS THIS SHEET TP13→TP18

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: FRACTIONAL ± 1/64
ANGLES ± 1°
TWO PLACE DECIMAL ± .010
THREE PLACE DECIMAL ± .005
DO NOT SCALE THIS DRAWING

MATERIAL

NEXT ASSEMBLY · USED ON · APPLICATION

DRAWN Michael Wigal 1/4/79 · CHECKED · DESIGN ENGINEER SAM SAWYER · PROJECT ENGINEER · CHIEF ENGINEER · MANUFACTURING · GENERAL MANAGER

tandy SYSTEMS DESIGN
2725 West Seventh Street Fort Worth, Texas 76107

TITLE: CPU MODULE MODEL II

SIZE B · DRAWING NO. 8000051 · REV D · SCALE · SHEET 8 OF 8

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	V. TERRY REVISED AND REDRAWNED	7-18-79	
	B	V. TERRY 1. ADDED TP14 AND R18 AND TP29	8-20-79	
D2	B1	1. ADDED CONNECTIONS AND REMOVED ARROW HEAD 2. ADDED PIN OUT	11-1-79	
C7		CONTINUED SHEET 2		

CONTINUED ON SECOND SHEET

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	26-4002
	26-4001
NEXT ASSEMBLY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: FRACTIONAL ± 1/64
ANGLES ± 1°
TWO PLACE DECIMAL ± .010
THREE PLACE DECIMAL ± .005
DO NOT SCALE THIS DRAWING
MATERIAL

		DATE
DRAWN	V. TERRY	7-18-79
CHECKED		DATE
DESIGN ENGINEER	SAM SAWYER	DATE 11/14/79
PROJECT ENGINEER		DATE 5 NOV 79
CHIEF ENGINEER		DATE
MANUFACTURING		DATE
GENERAL MANAGER		DATE

tandy SYSTEMS DESIGN
2725 West Seventh Street Fort Worth, Texas 76107

TITLE: FDC-PRINTER INTERFACE BOARD

SIZE D | DRAWING NO. 8000042 | REV 01 | SCALE 1/2A | SHEET 1 OF 2

CONTINUED ON SHEET 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
4C 7C	C	1. ADDED U37 R54 C35 2. ADDED R38	12-3-79	

JUMPER A TO B IF CPU CLOCK = 4 MHZ
JUMPER B TO C IF CPU CLOCK = 2 MHZ

CLOCK DIVIDE BY 2

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: FRACTIONAL ± 1/64
ANGLES ± 1°
TWO PLACE DECIMAL ± .010
THREE PLACE DECIMAL ± .005
DO NOT SCALE THIS DRAWING

MATERIAL

NEXT ASSEMBLY | USED ON
APPLICATION

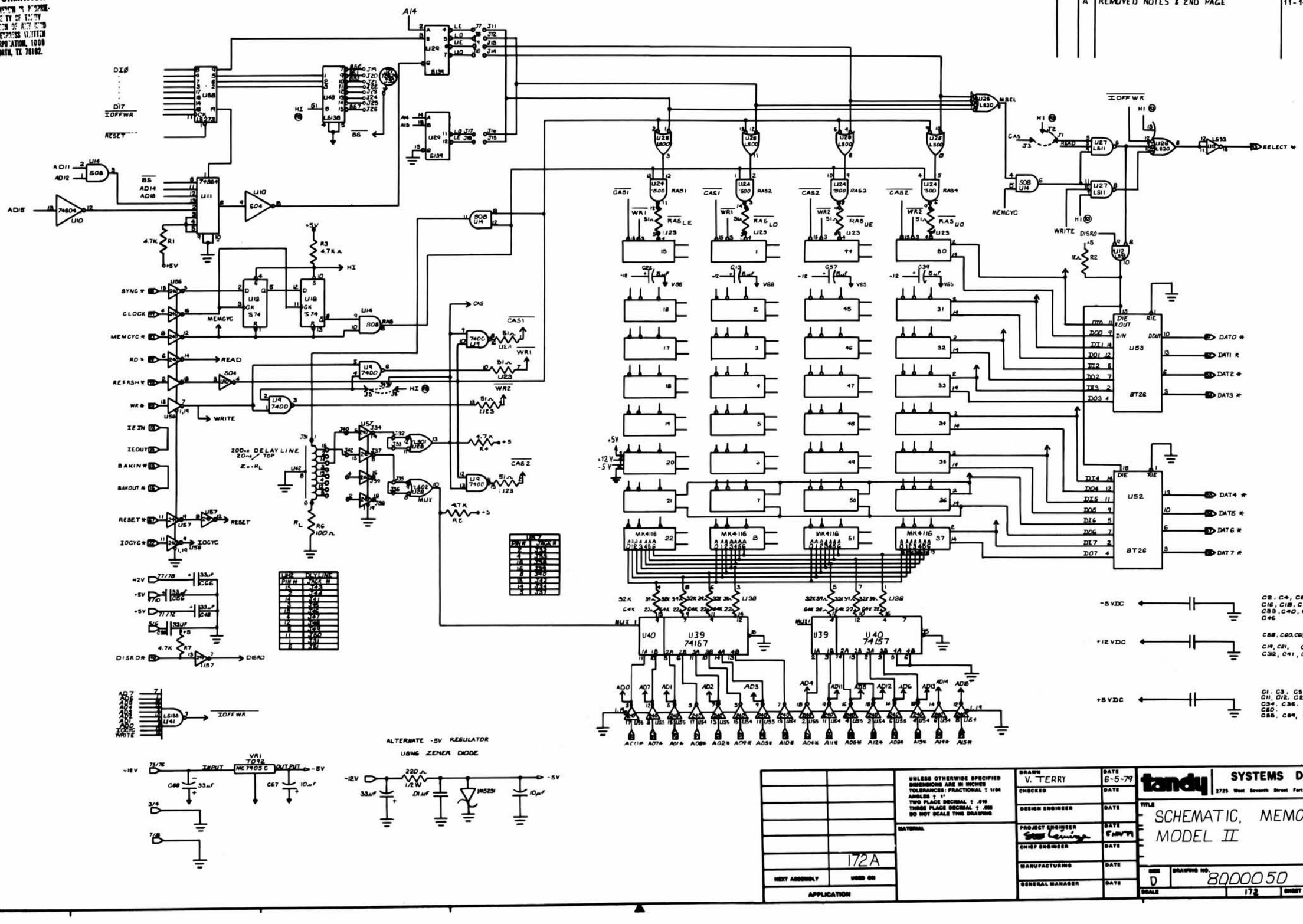
DRAWN	V. TERRY	7-18-79
CHECKED		
DESIGN ENGINEER	SAM SAWYER	11/20/78
PROJECT ENGINEER		
CHIEF ENGINEER		
MANUFACTURING		
GENERAL MANAGER		

tandy SYSTEMS DESIGN
2725 West Seventh Street Fort Worth, Texas 76107

TITLE: FDC PRINTER INTERFACE BOARD

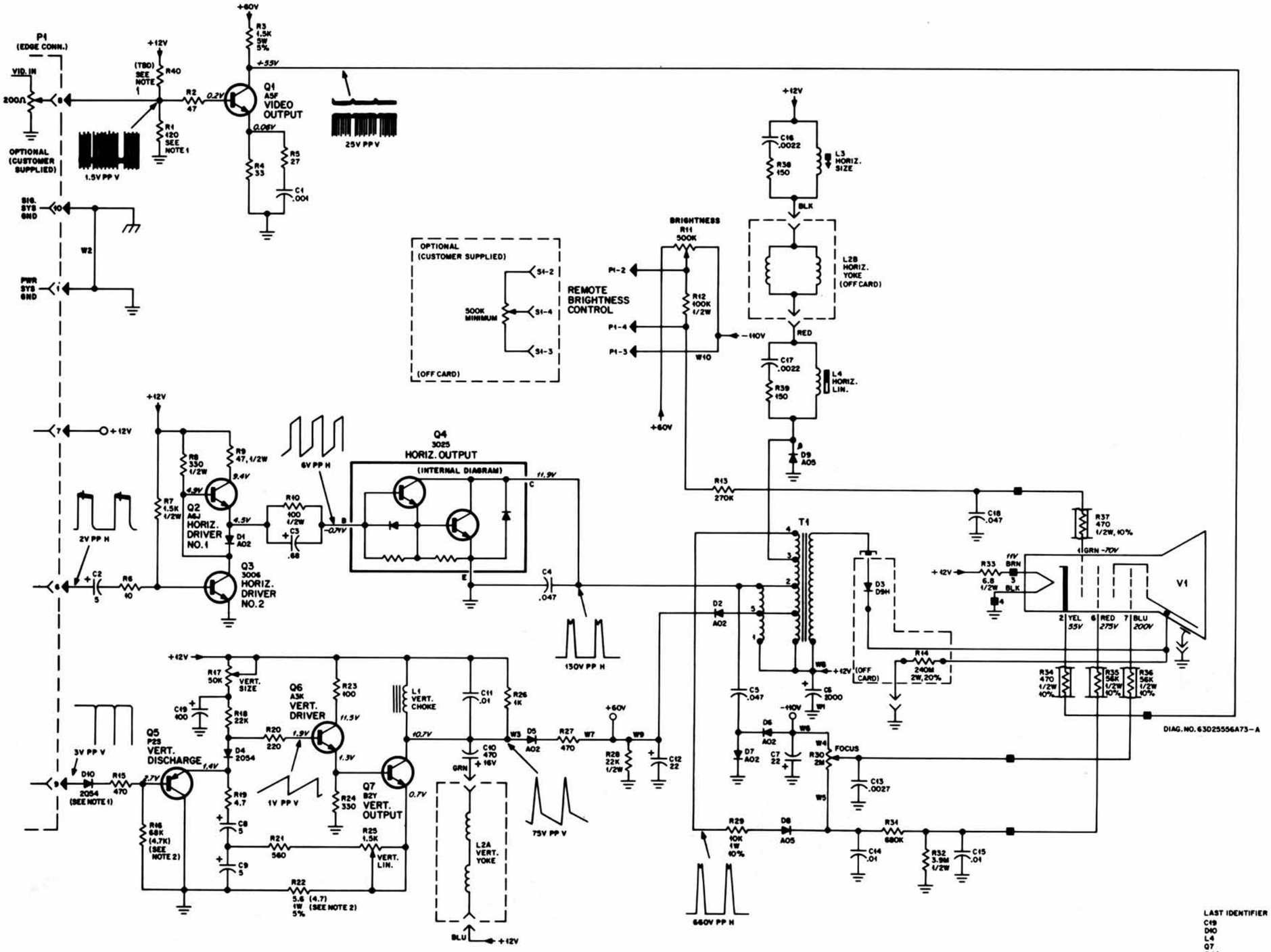
SIZE D | DRAWING NO. 800042 | REV C
SCALE 1/1 | SHEET 2 OF 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REMOVED NOTES & 2ND PAGE	11-1-79	



		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: FRACTIONAL ± 1/64 ANGLES ± 1° TWO PLACE DECIMAL ± .010 THREE PLACE DECIMAL ± .005 DO NOT SCALE THIS DRAWING	DRAWN V. TERRY	DATE 6-5-79	tandy SYSTEMS DESIGN 2725 West Seventh Street Fort Worth, Texas 76107
			CHECKED	DATE	TITLE SCHEMATIC, MEMORY MODEL II
		MATERIAL	DESIGN ENGINEER	DATE	
			PROJECT ENGINEER	DATE 6 NOV 79	
	172A		CHIEF ENGINEER	DATE	SIZE D DRAWING NO. 8000050 REV A
NEXT ASSEMBLY	USED ON		MANUFACTURING	DATE	SCALE 172 SHEET 1 OF 1
APPLICATION			GENERAL MANAGER	DATE	

8000050



NOTES:

UNLESS OTHERWISE SPECIFIED:
ALL CAPACITORS ARE IN MICROFARADS
RESISTORS ARE 1/4W, 5%.

DENOTES RESISTOR IN CRT SOCKET LEAD.

CIRCUIT CARD EDGE CONNECTION

MALE PLUG CONNECTION

FEMALE SOCKET CONNECTION

COMPONENTS ENCLOSED BY DASHED LINES ARE MOUNTED OFF CIRCUIT CARD.

■ REPRESENTS CONNECTION TO OFF CIRCUIT CARD LOCATION.

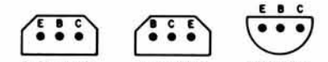
1. PART NOT IN ALL SETS.
2. LESSER VALUES INSTALLED WHEN D10 IS USED.

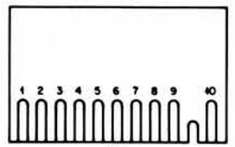
H.V. CONNECTOR

VOLTAGES MEASURED WITH CONTROLS SET FOR NOMINAL OPERATION; INPUT SIGNALS AS SHOWN.

DC VOLTAGES MEASURED WITH 1% DVM.

WAVEFORMS TAKEN WITH 10MHZ OSCILLOSCOPE REFERENCED TO SIGNAL GROUND, AND SYNCED AT VERTICAL OR HORIZONTAL RATE AS INDICATED.





1. POWER GND
2. REMOTE BRIGHT HIGH
3. REMOTE BRIGHT LOW
4. REMOTE BRIGHT WIPER
5. N.C.
6. HORIZONTAL DRIVE
7. +12V DC B+
8. VIDEO
9. VERTICAL DRIVE
10. SIGNAL GND

LAST IDENTIFIER
C19
D10
L4
Q7
R40
T1
W10

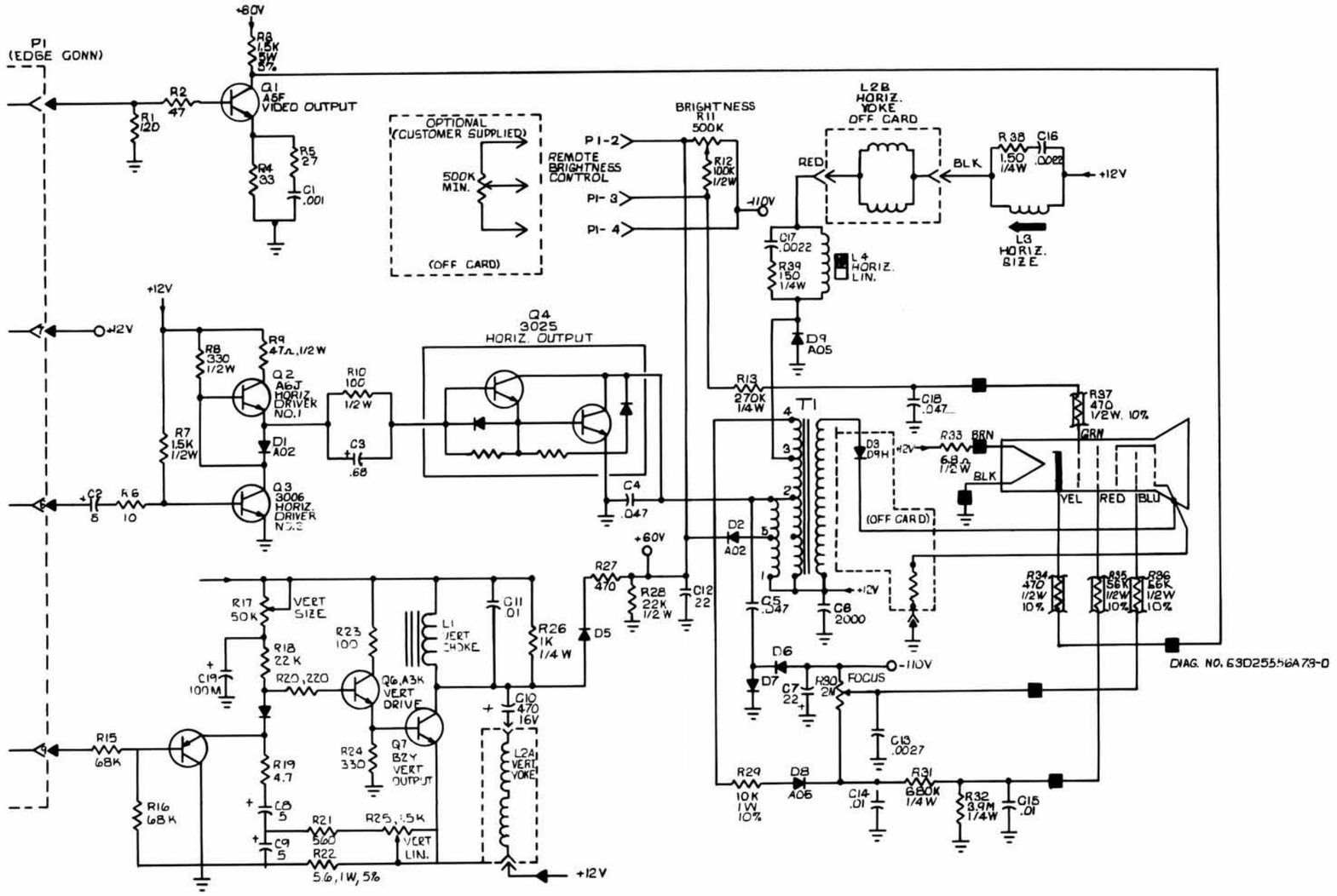
tandy SYSTEMS DESIGN
2725 West Seventh Street Fort Worth, Texas 76107

TITLE: VIDEO DISPLAY

SIZE: D | DRAWING NO: 8000049 | REV:

SCALE: | SHEET 1 OF 2

MOTOROLA INC.
Display Systems
M3970-191
63025556A73



DWG NO	REV
8000049	
SCALE	SHEET 2 OF 2

RADIO SHACK, A DIVISION OF TANDY CORPORATION

U.S.A.: FORT WORTH, TEXAS 76102
CANADA: BARRIE, ONTARIO L4M 4W5

TANDY CORPORATION

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